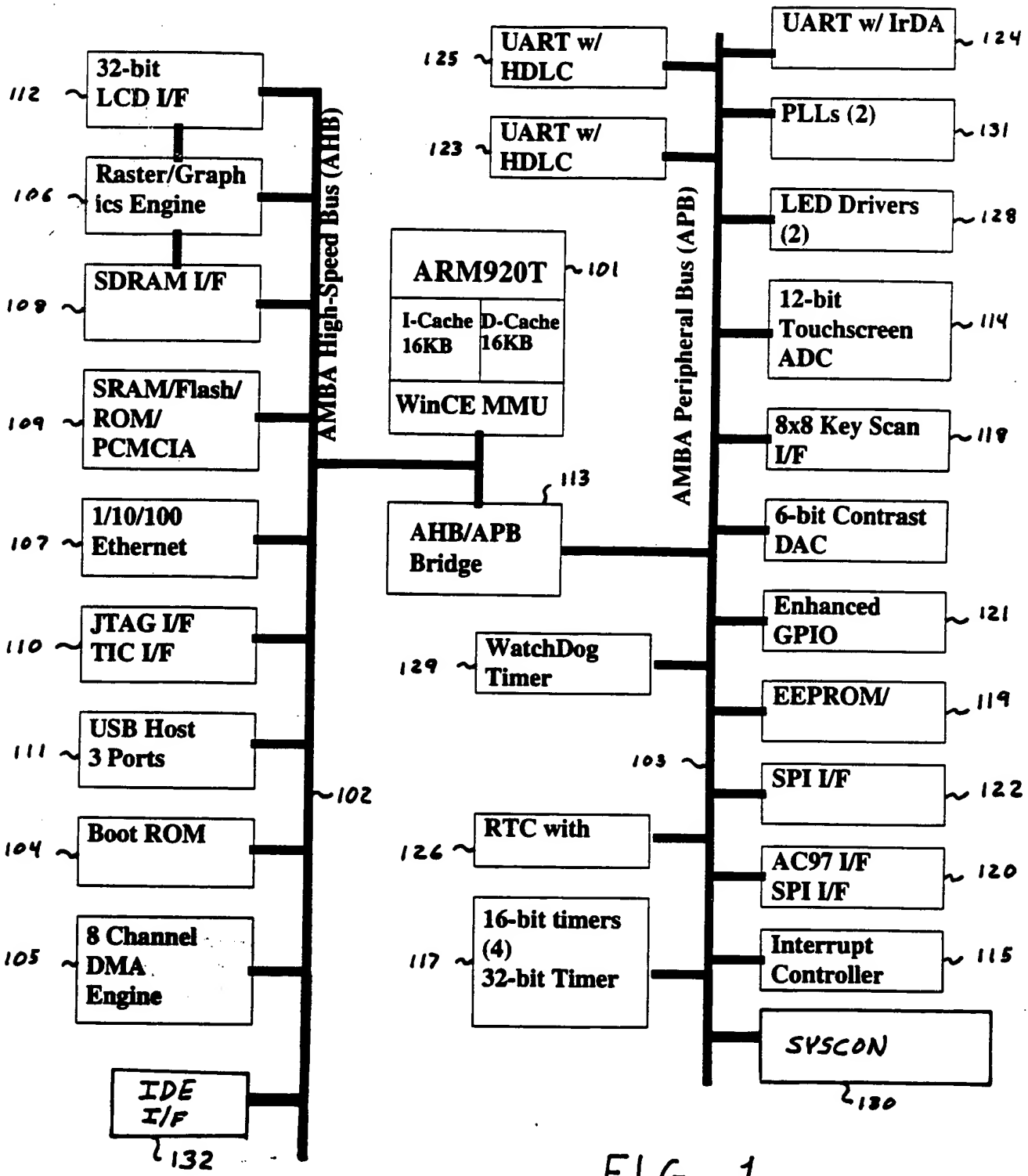
1042-EP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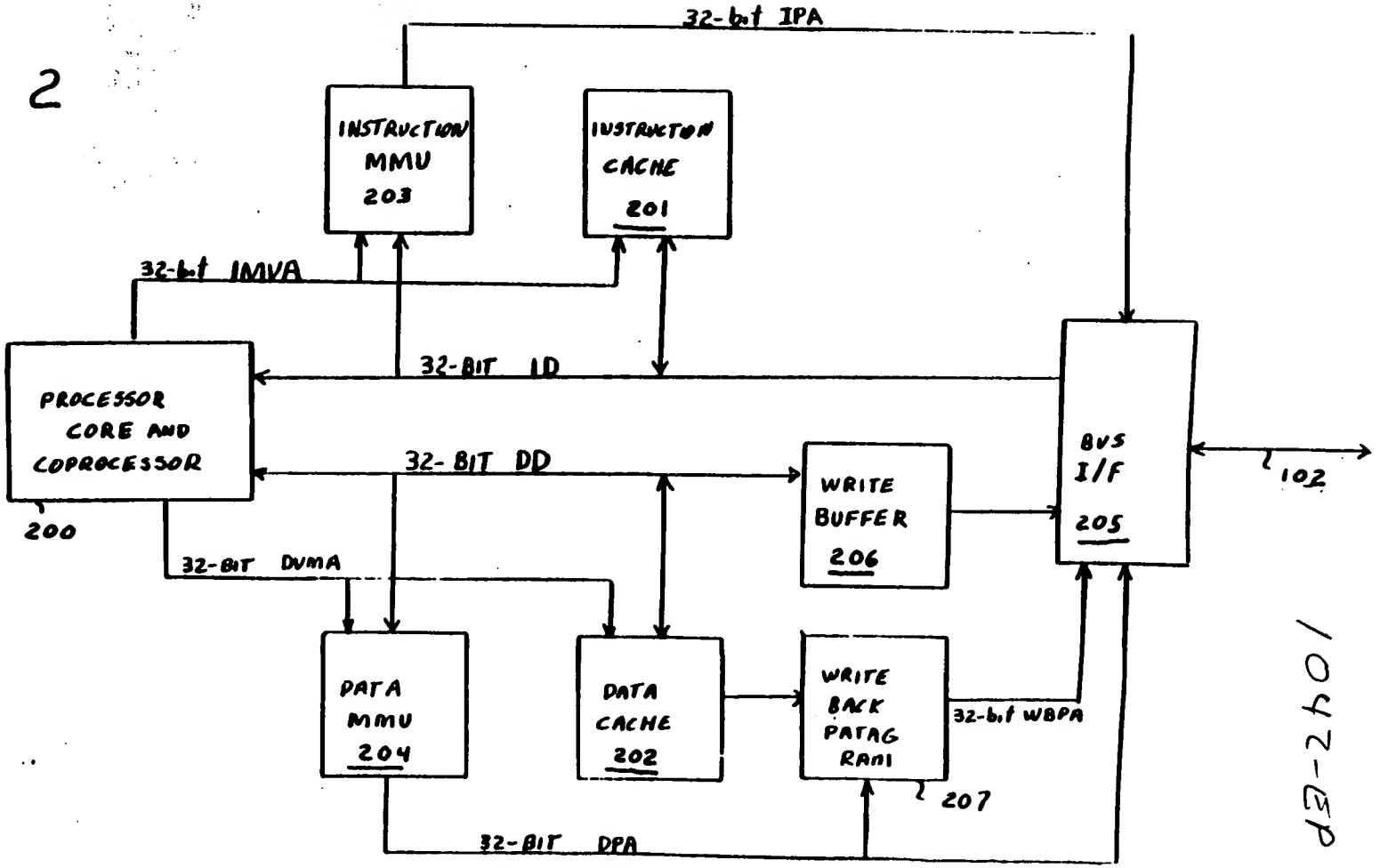
32-bit LCD I/F
112
Raster/Graphics Engine
106
SDRAM I/F
108
SRAM/Flash/ ROM/ PCMCIA
109
1/10/100 Ethernet
107
JTAG I/F TIC I/F
110
USB Host 3 Ports
111
Boot ROM
104
8 Channel DMA Engine
105
IDE I/F
132
AMBA High-Speed Bus (AHB)
102
ARM920T
101
I-Cache 16KB
D-Cache 16KB
WinCE MMU
AHB/APB Bridge
113
AMBA Peripheral Bus (APB)
103
UART w/ HDLC
125
UART w/ HDLC
123
WatchDog Timer
129
RTC with
126
16-bit timers (4) 32-bit Timer
117
UART w/ IrDA
124
PLLs (2)
131
LED Drivers (2)
128
12-bit Touchscreen ADC
114
8x8 Key Scan I/F
118
6-bit Contrast DAC
Enhanced GPIO
121
EEPROM/
119
SPI I/F
122
AC97 I/F SPI I/F
120
Interrupt Controller
115
SYSCON
130

FIG. 1

006090 "6591656D

FIG. 2



03-2401

1042-EP

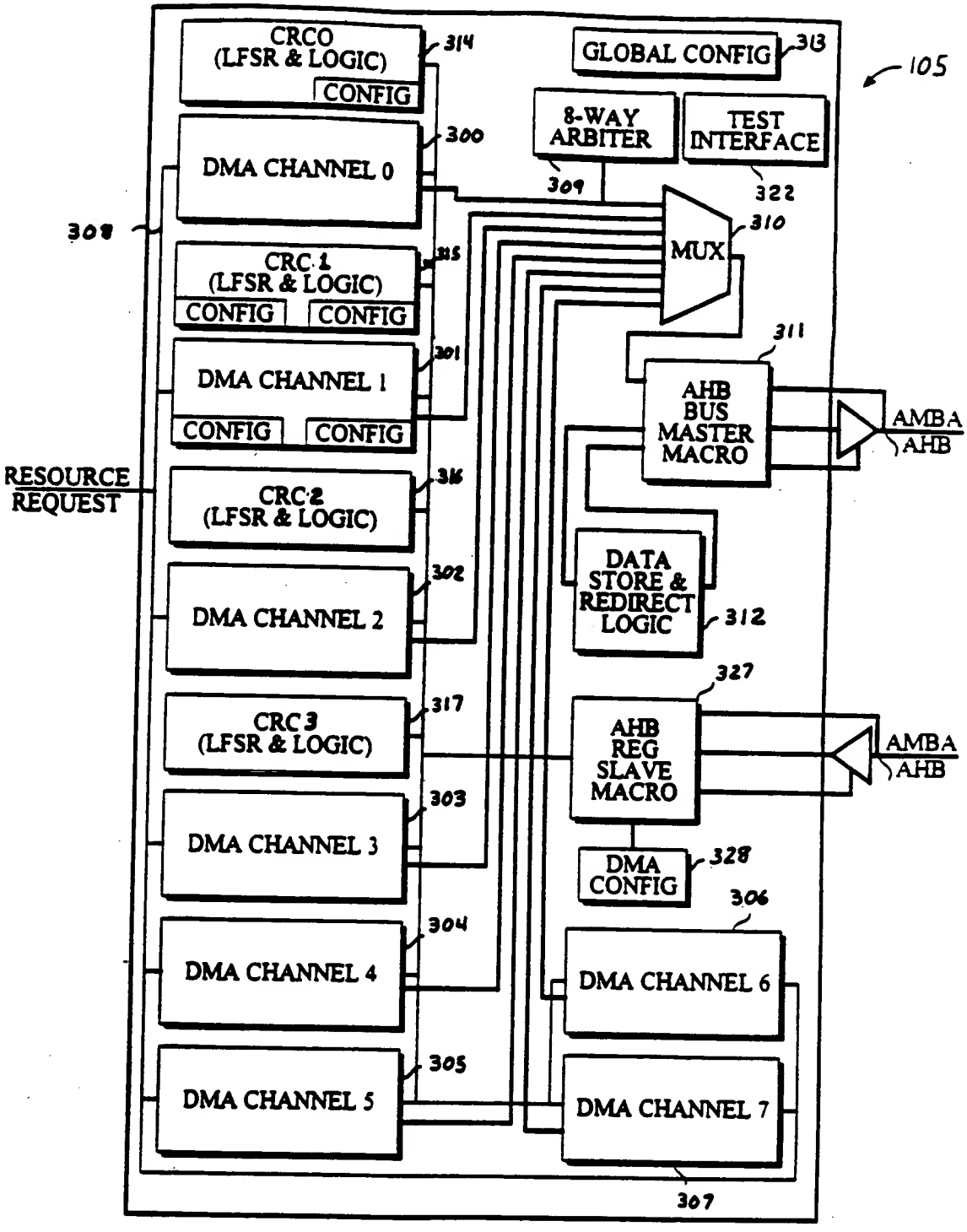


Fig. 3A

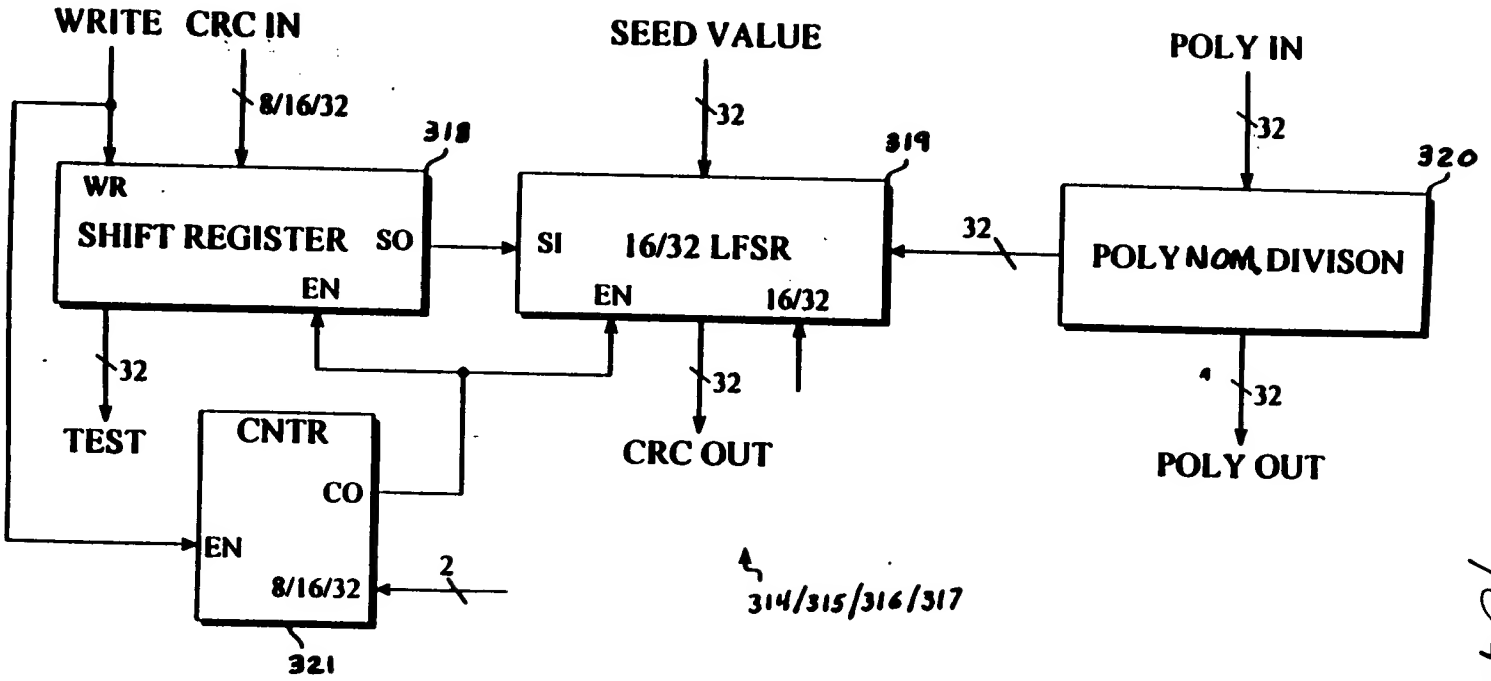


Fig. 3B

10/97-EP

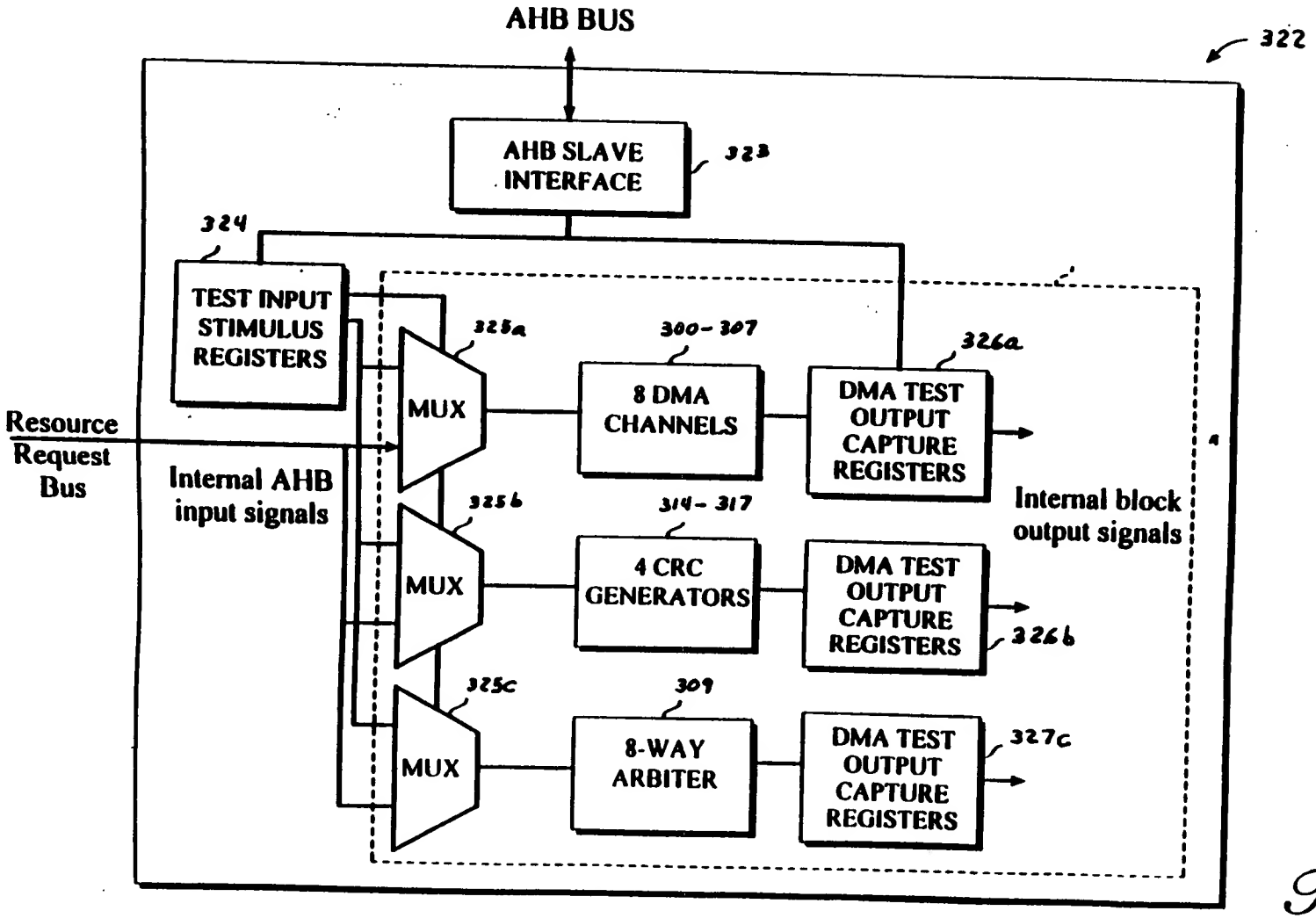


Fig. 3C

1042-EP

006090 "6591659

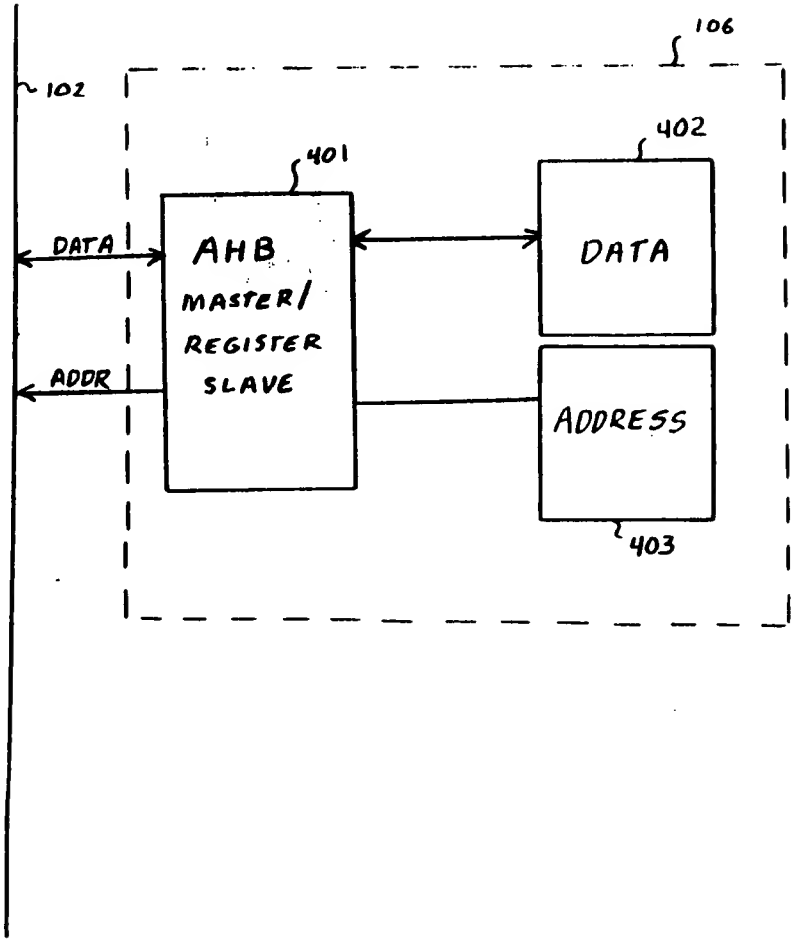


FIG. 4A

D3-2401

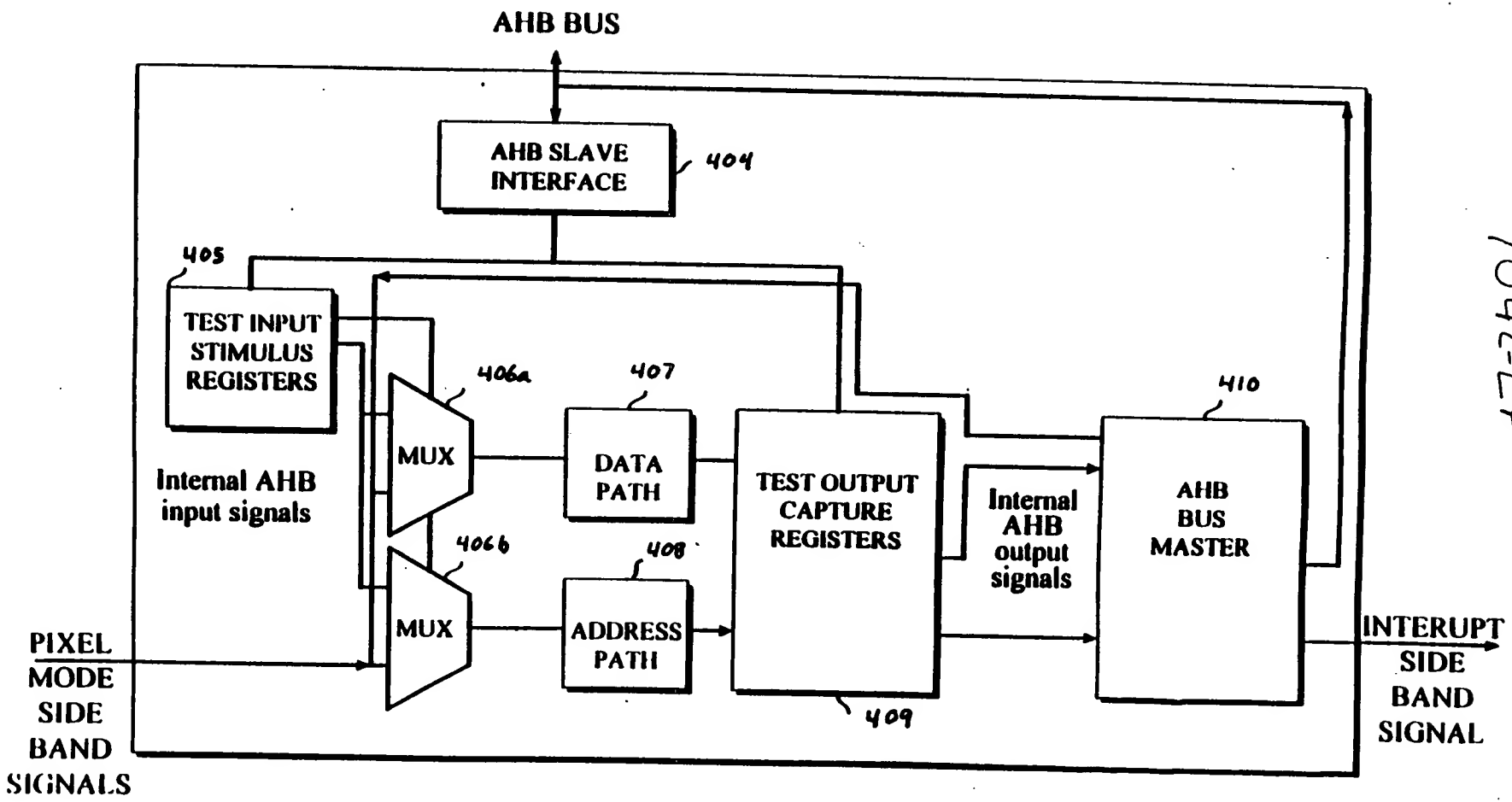
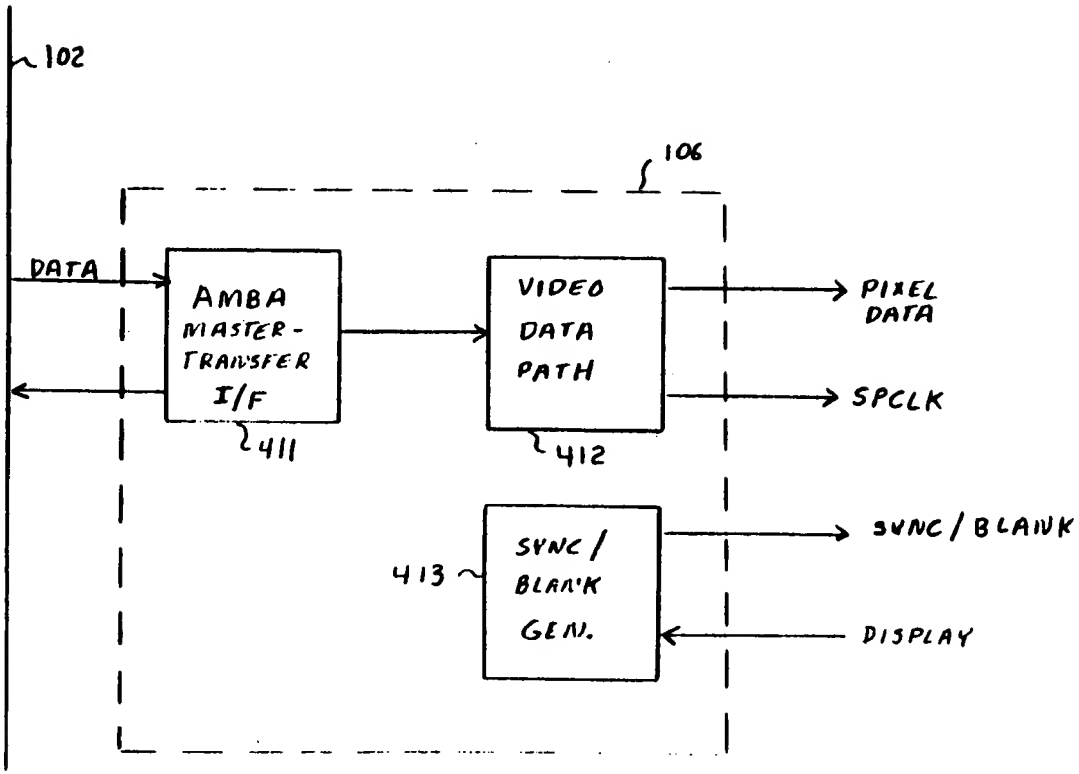


Fig. 4B

042-EP 01



1042-EP

FIG. 4C

1042-EP

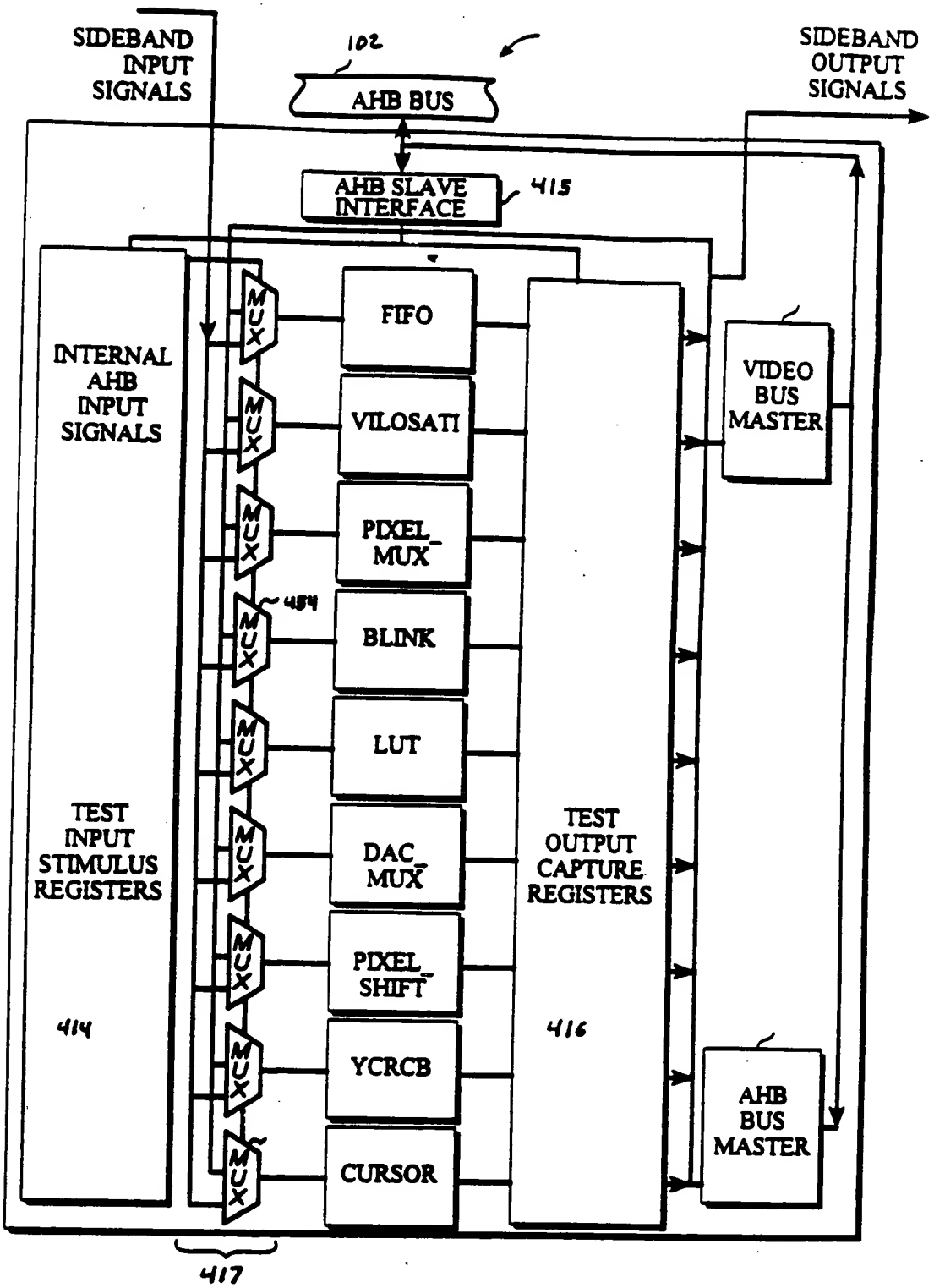


Fig. 4D

1042-EP

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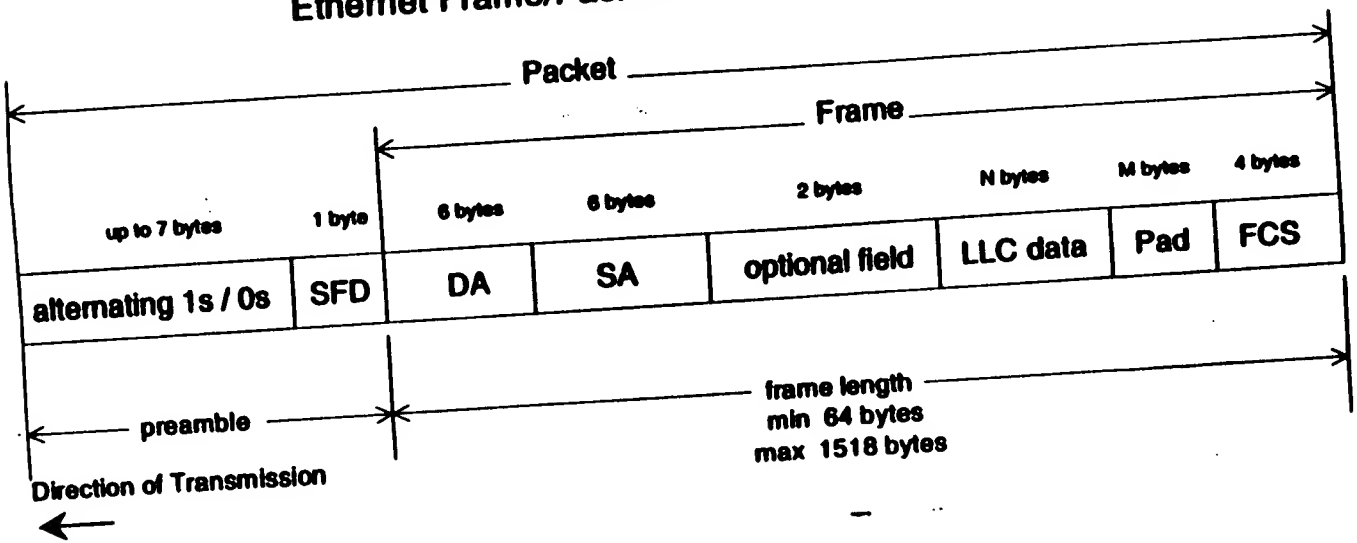


FIG. 5A

09591659 .060900

0060901;6597659D

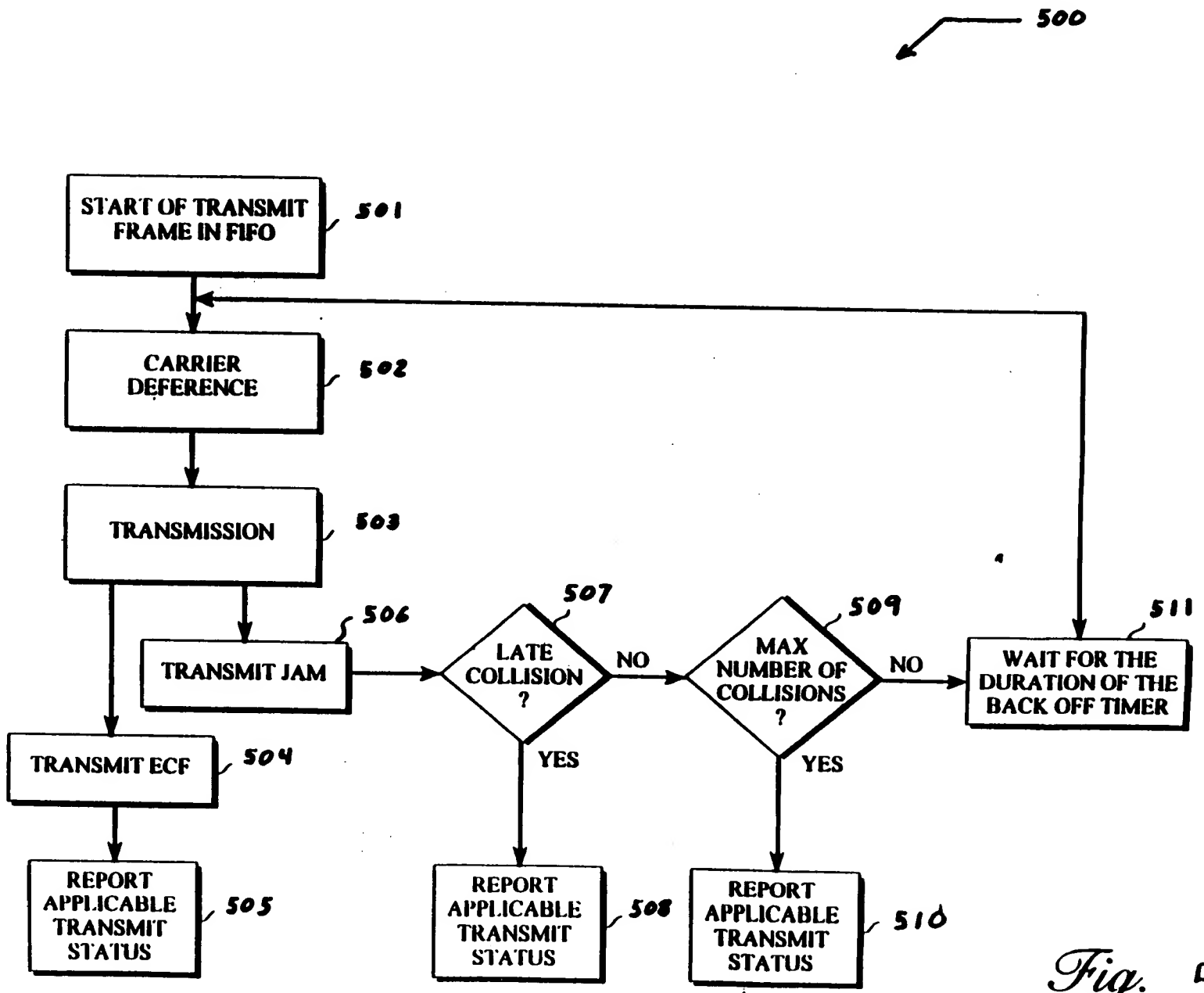


Fig. 5B

10942-2401

006090 6591659

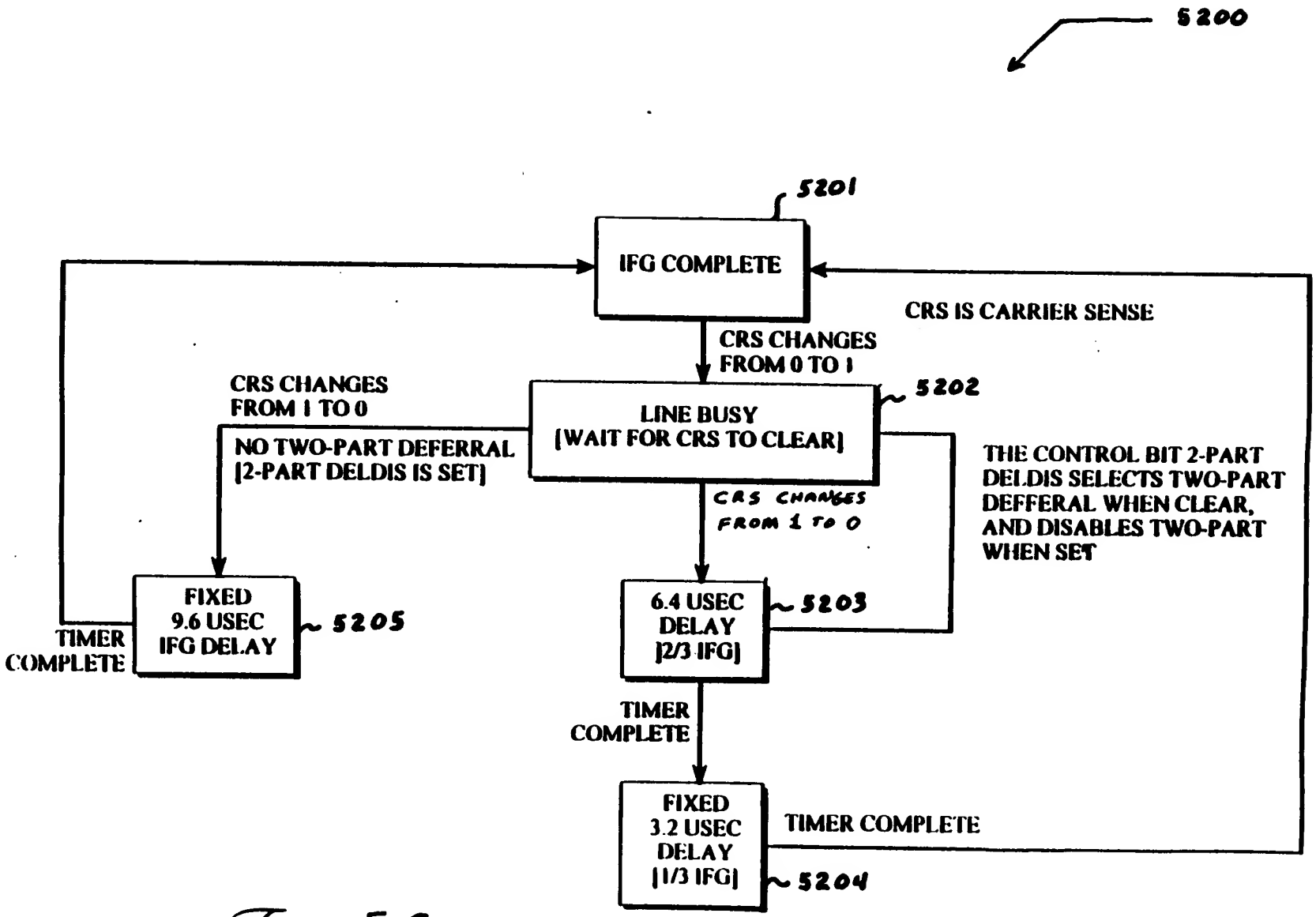
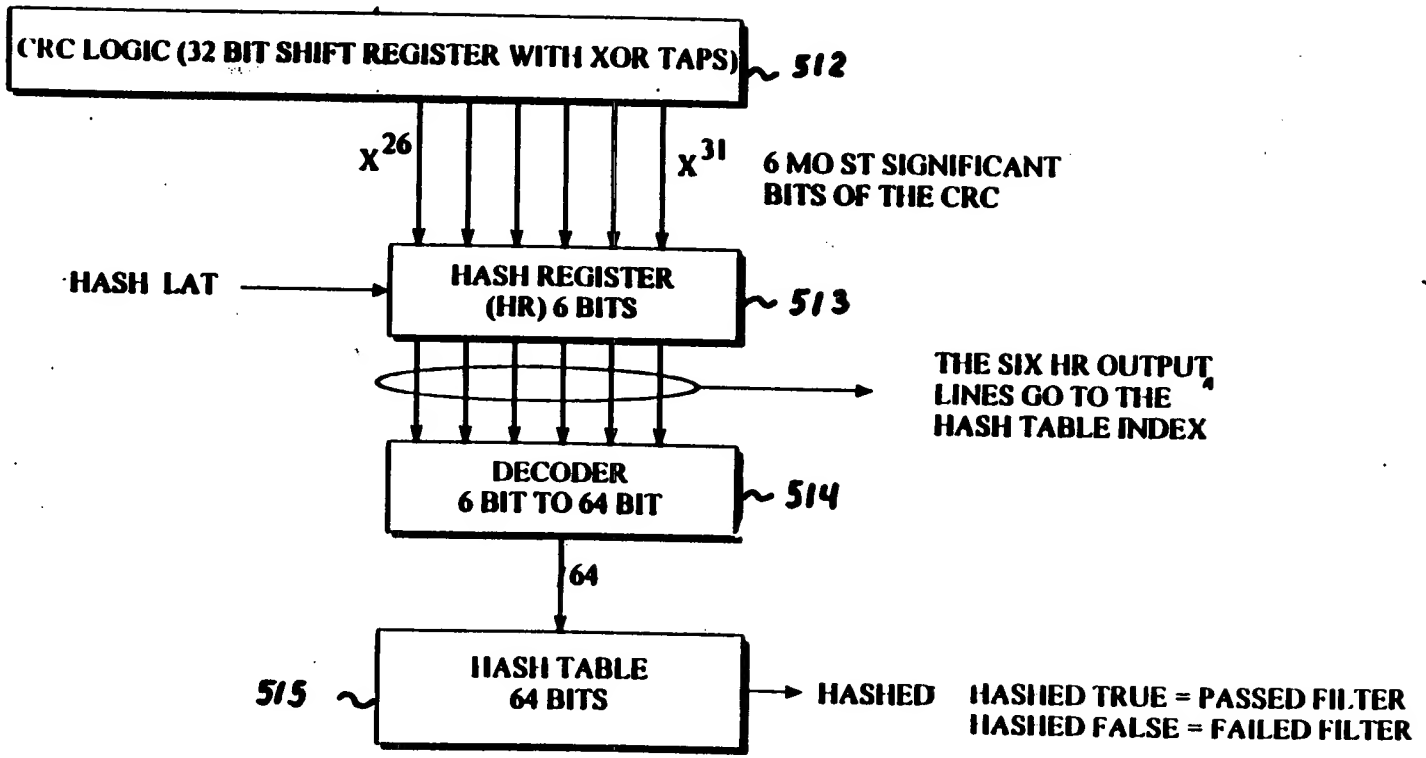


Fig. 5C

DS-2401

0060901 6597560



43-2401

Fig. 5D

1042-EP

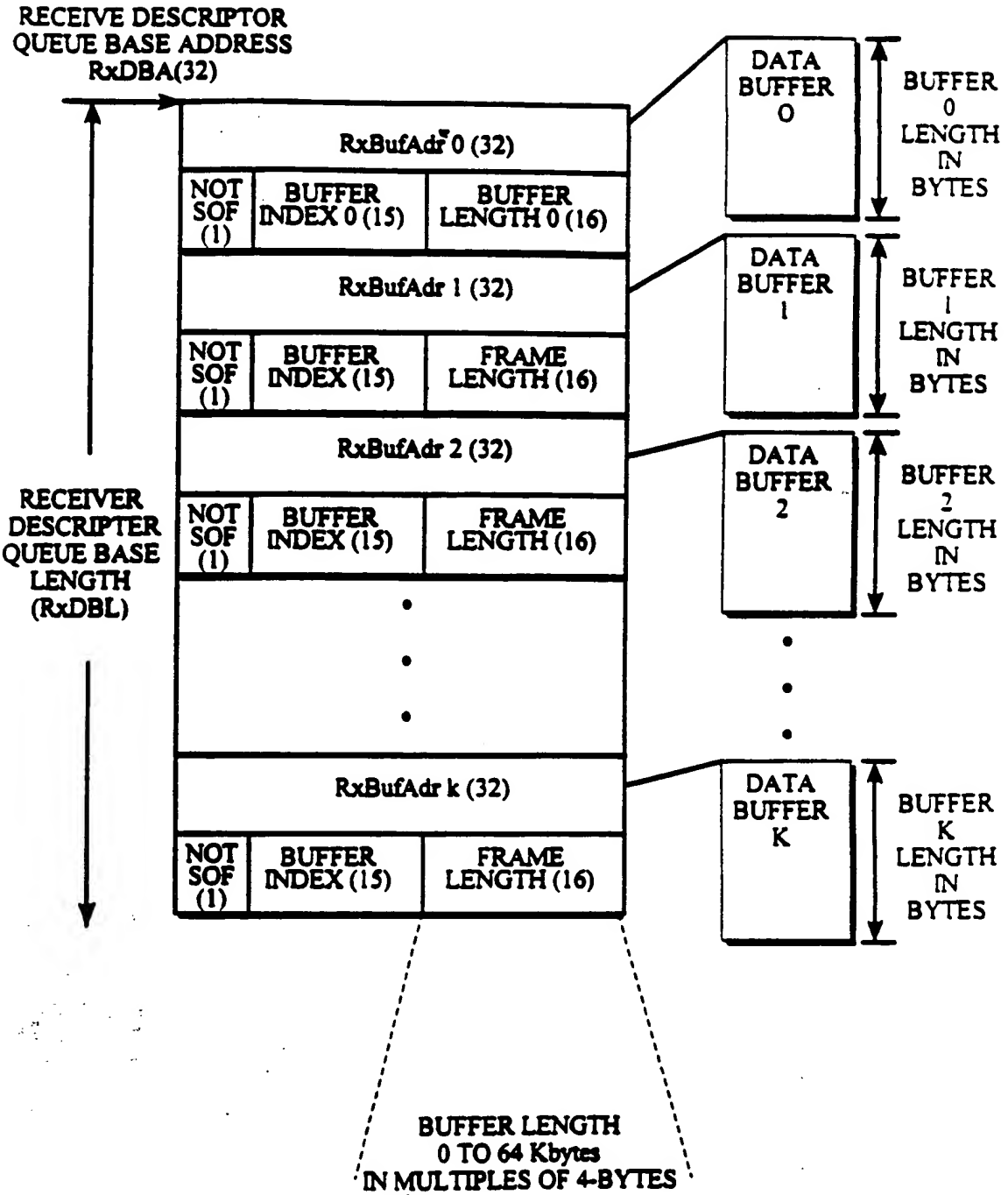


Fig. 5E

1042-EP

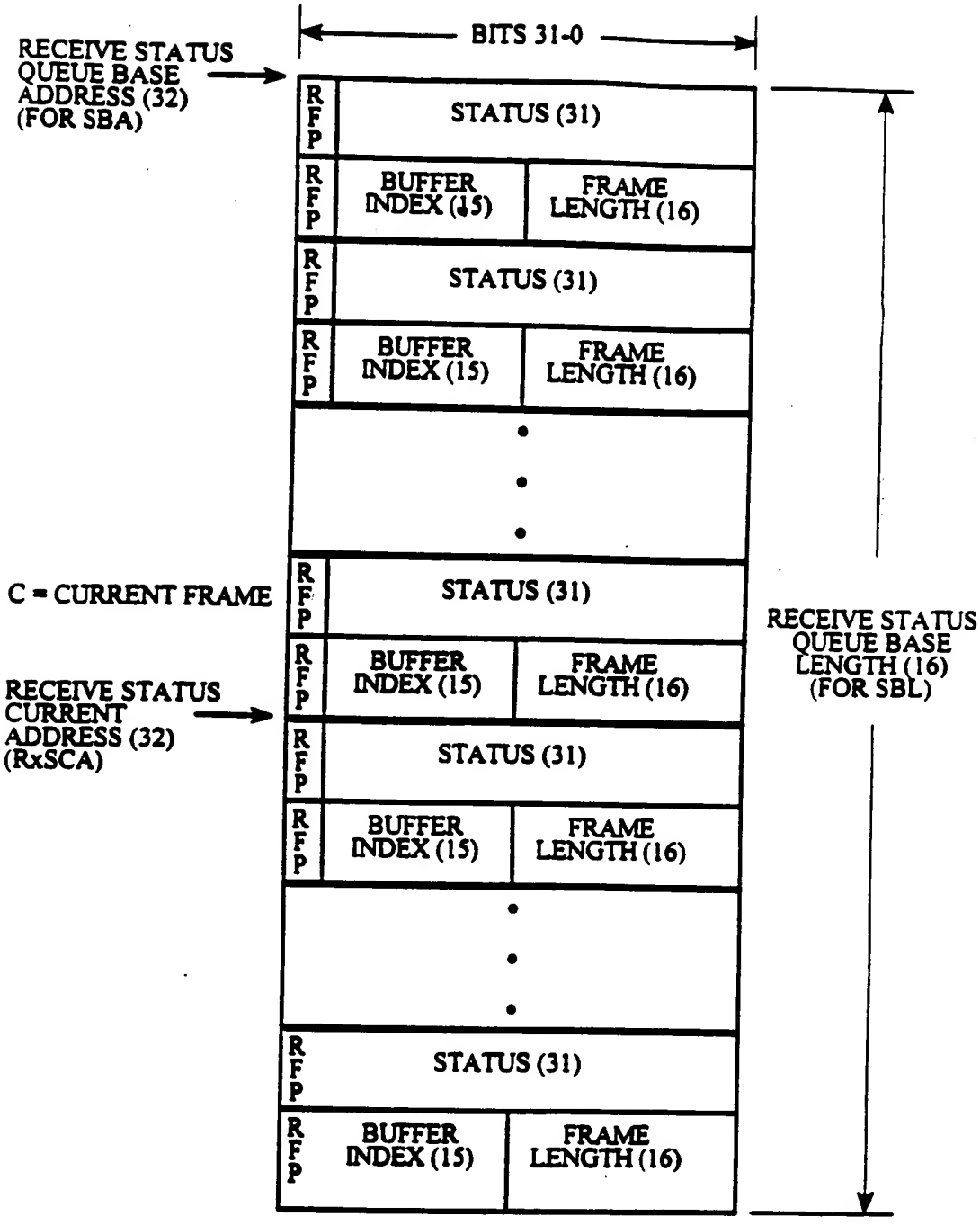


Fig. 5F

1042-EP

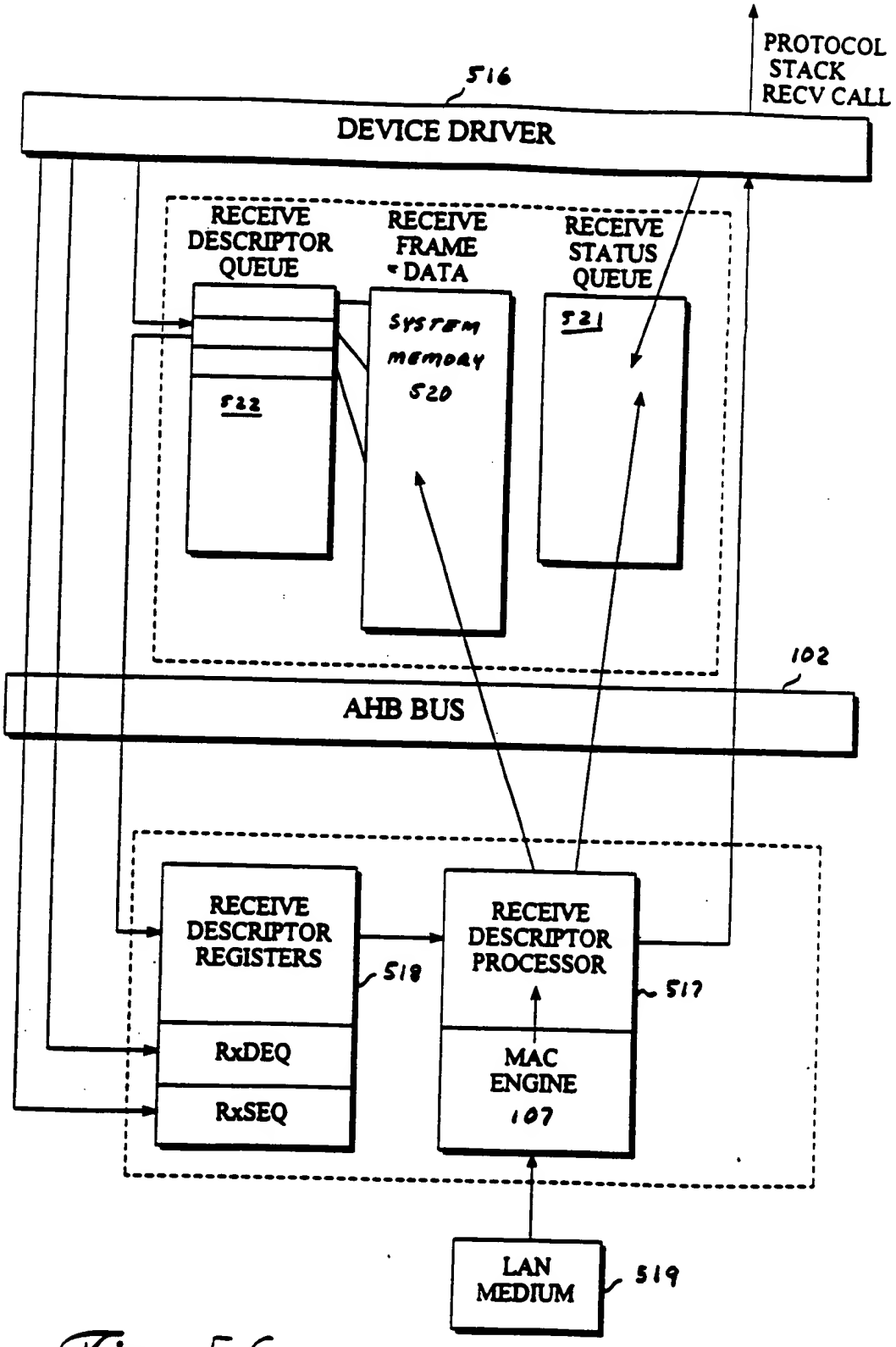


Fig. 5G

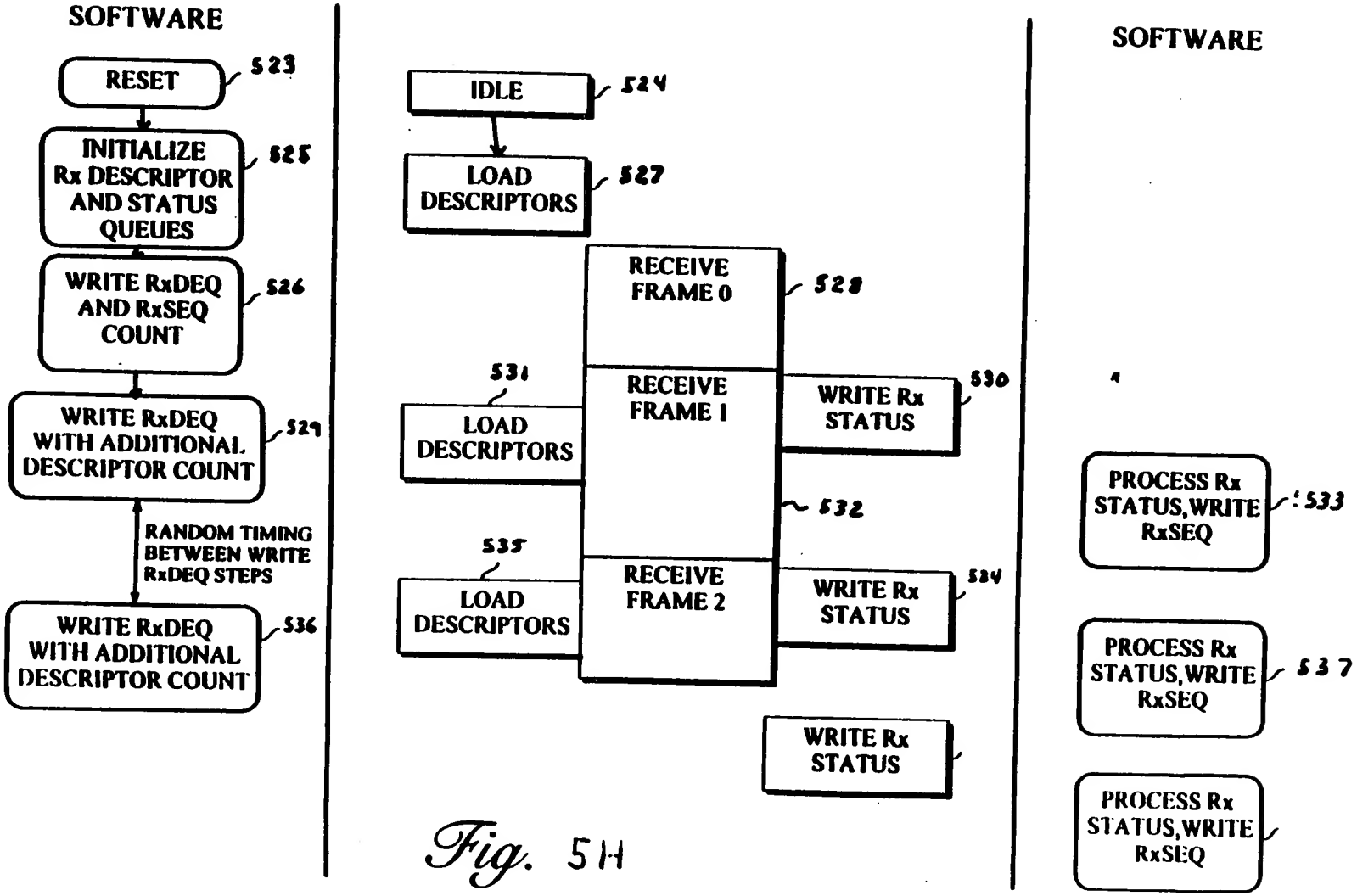


Fig. 5H

IE-2401-EP

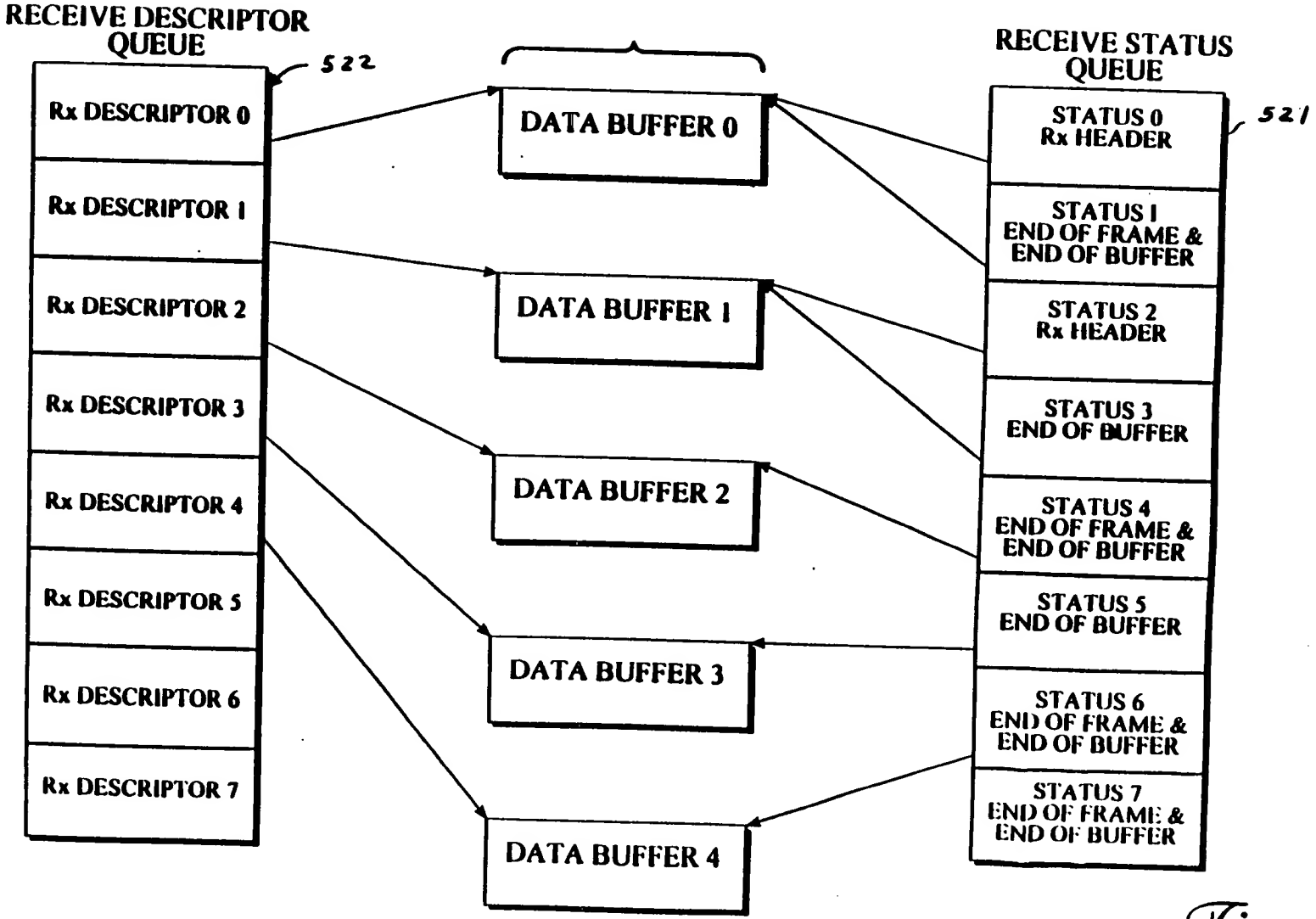


Fig. 51

1042-EP

1042-EP 5

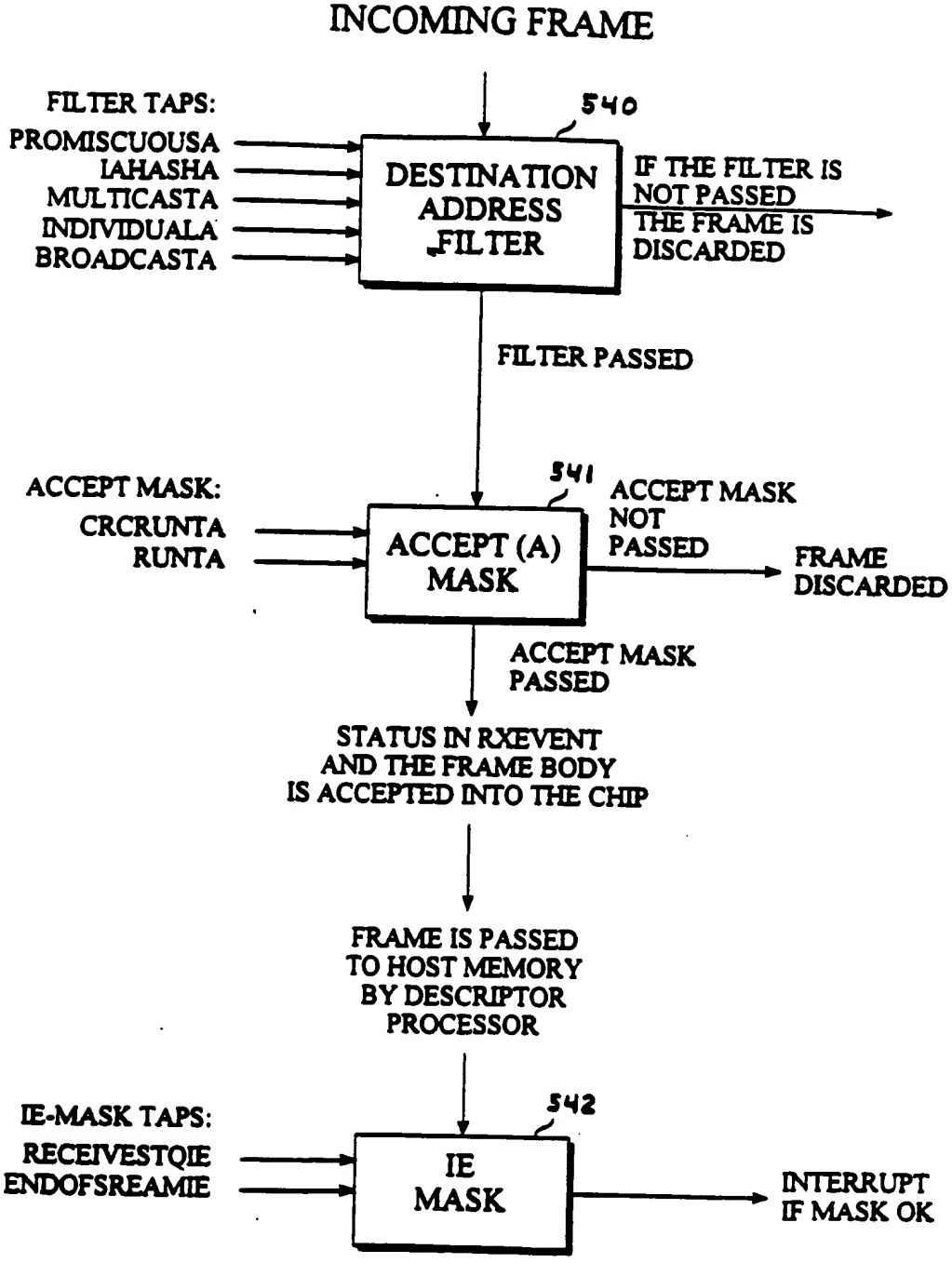


Fig. 5J

006090 6991e960

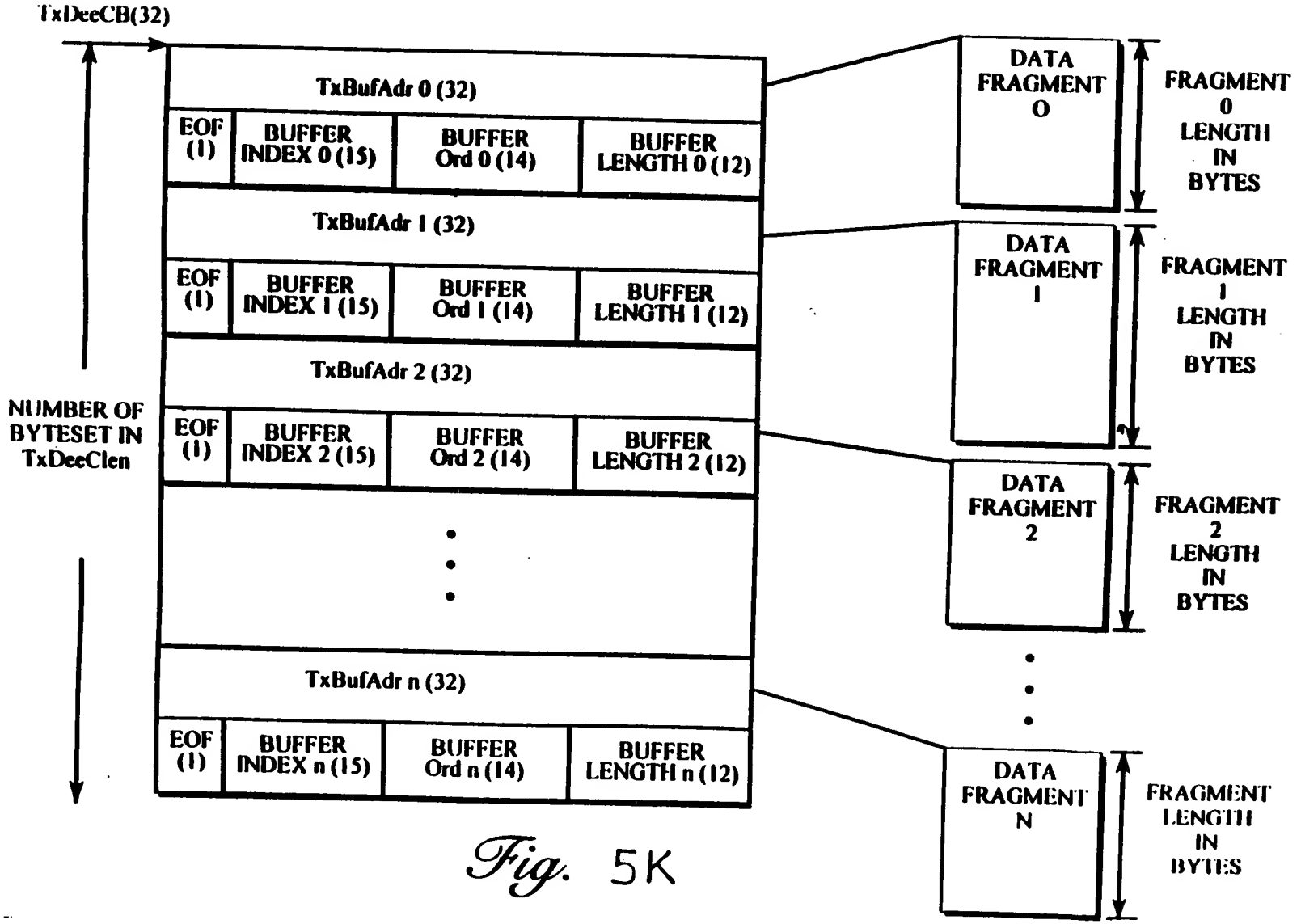


Fig. 5K

93-2601

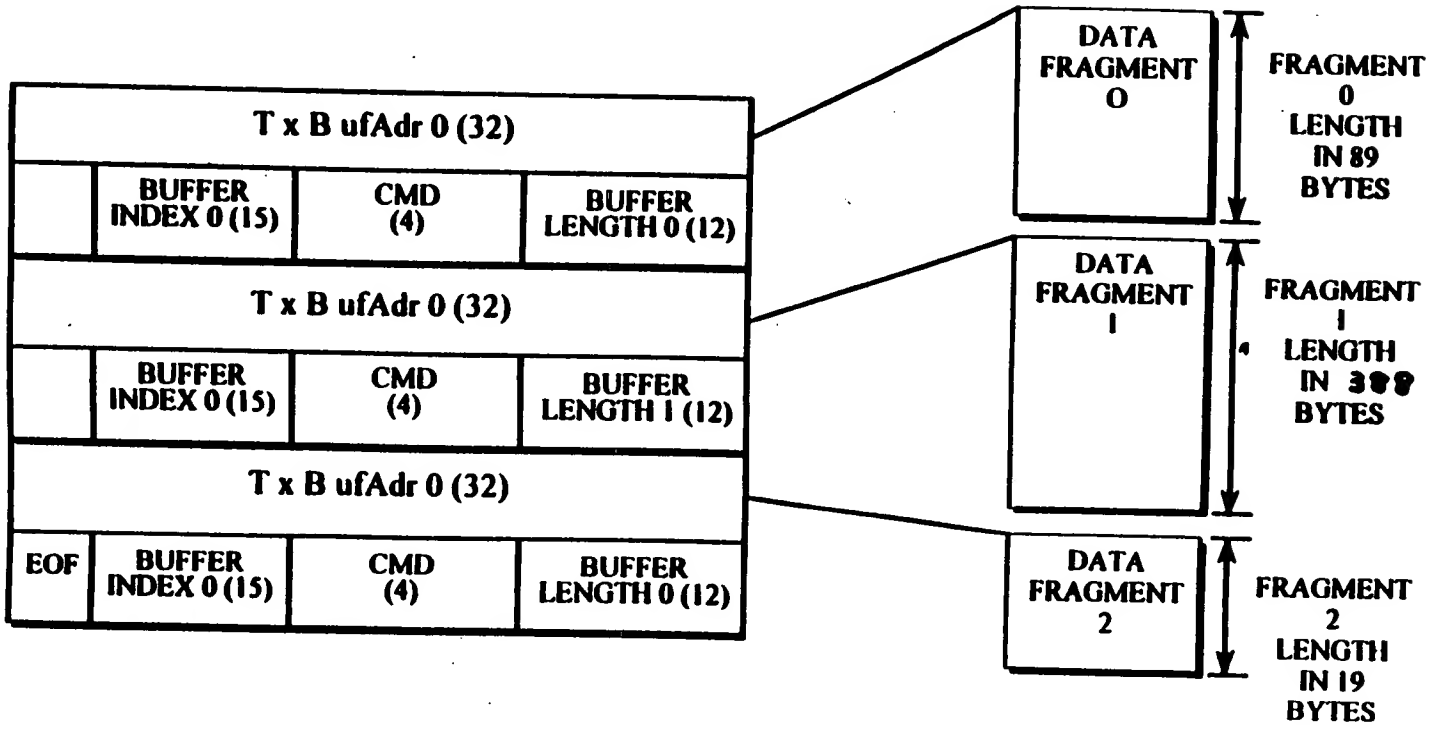


Fig. 5L

1092-E0

1042-EP

TRANSMIT STATUS QUEUE

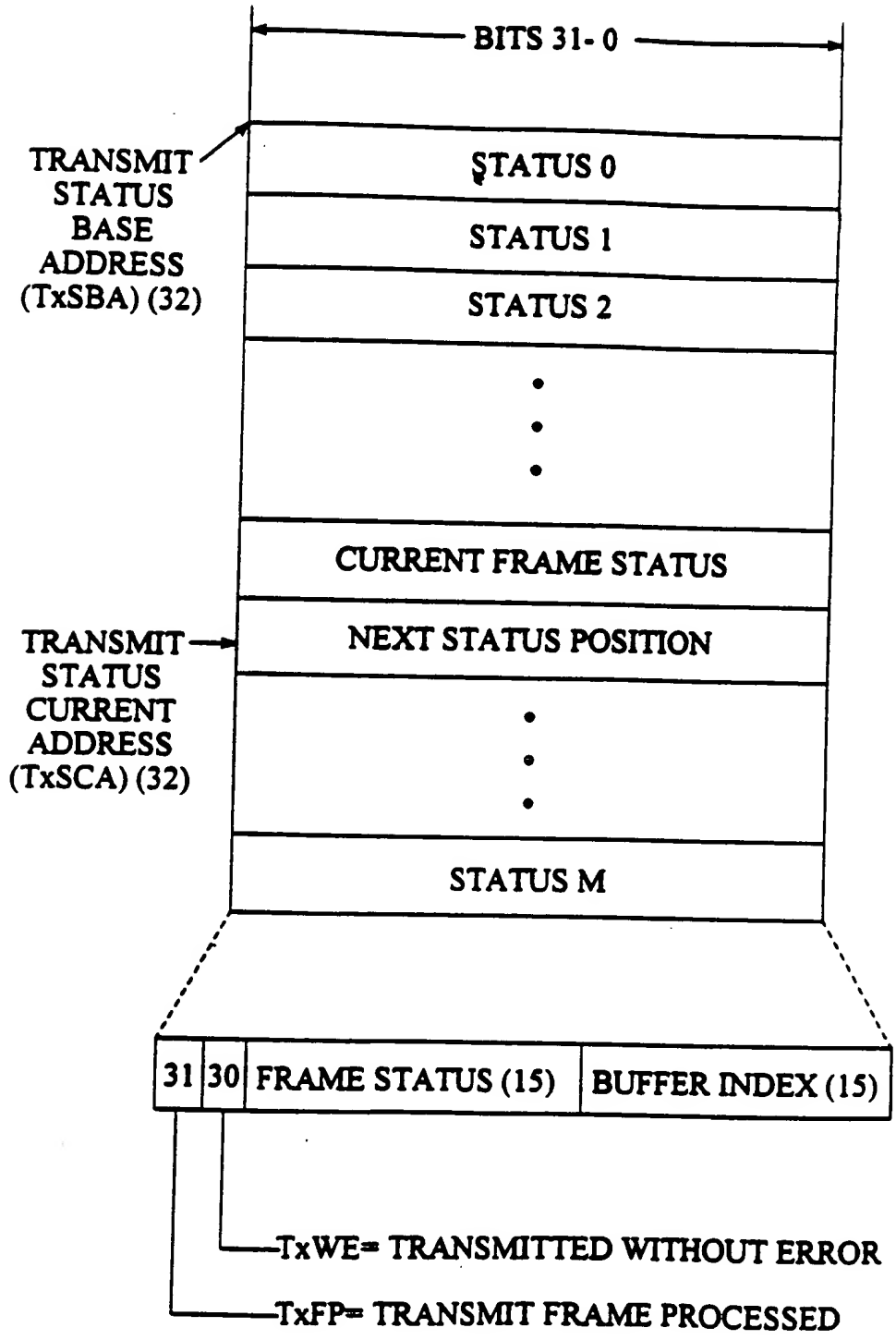


Fig. 5M

1042-EP

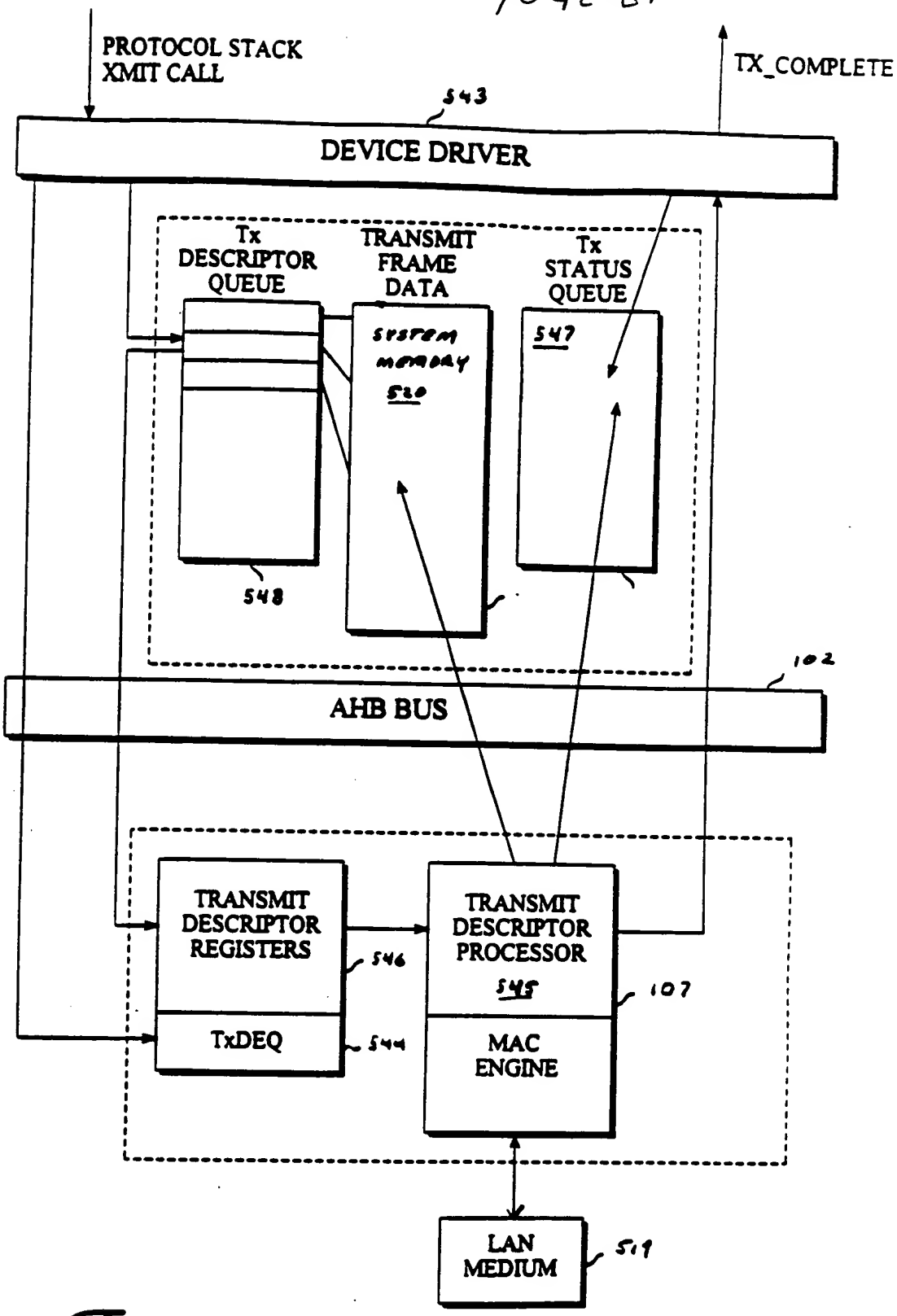


Fig. 5N

1042-ED

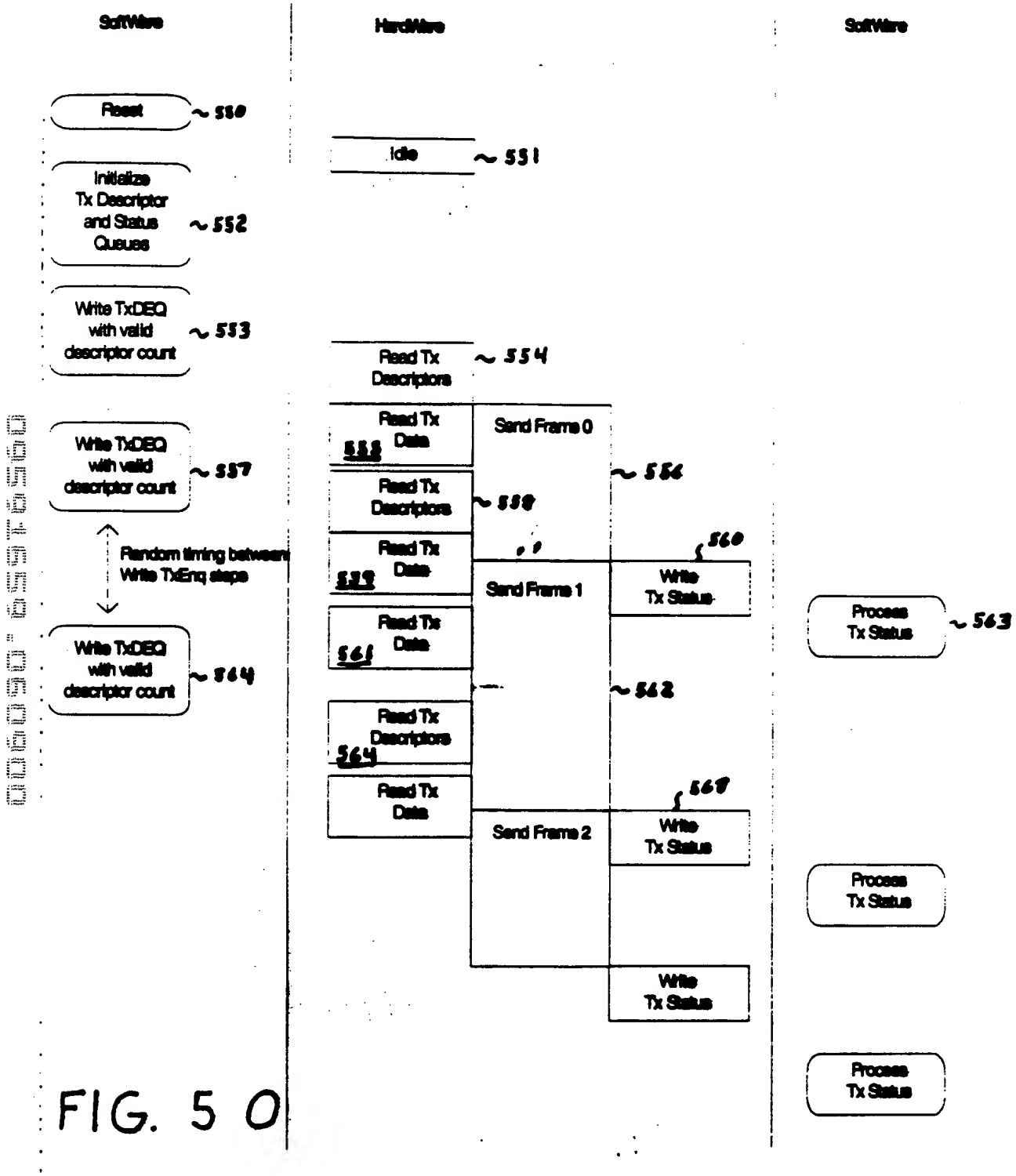


FIG. 5 0

006090 6997696O

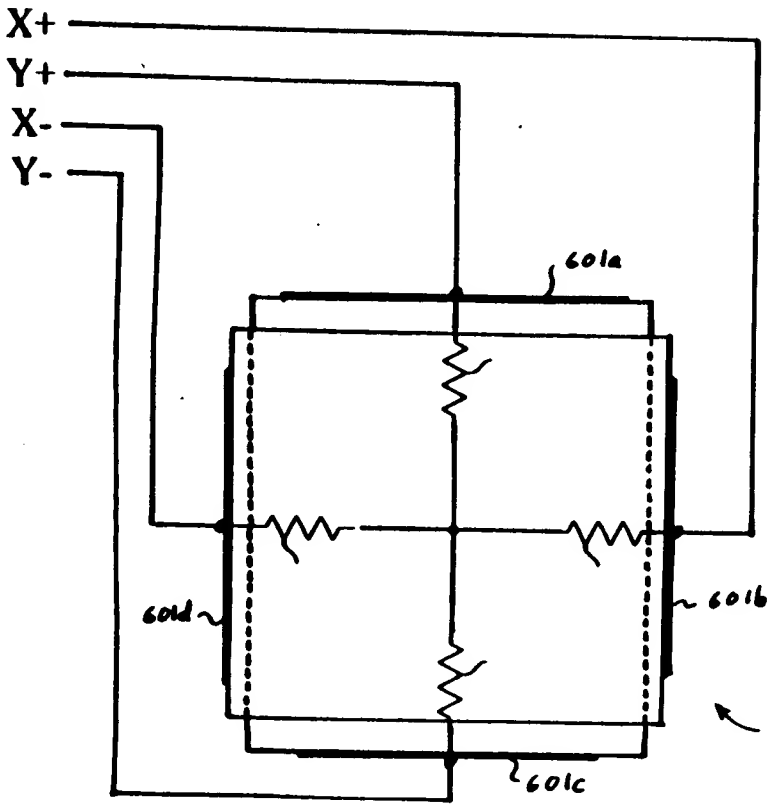


Fig. 6A

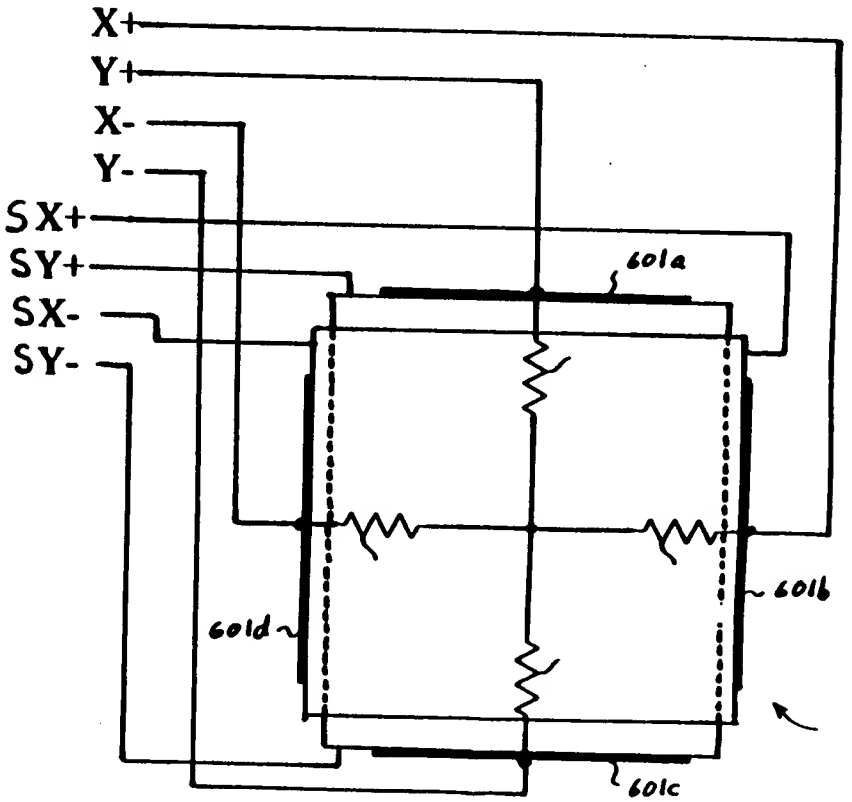


Fig. 6D

D-2401

006090 6597e560

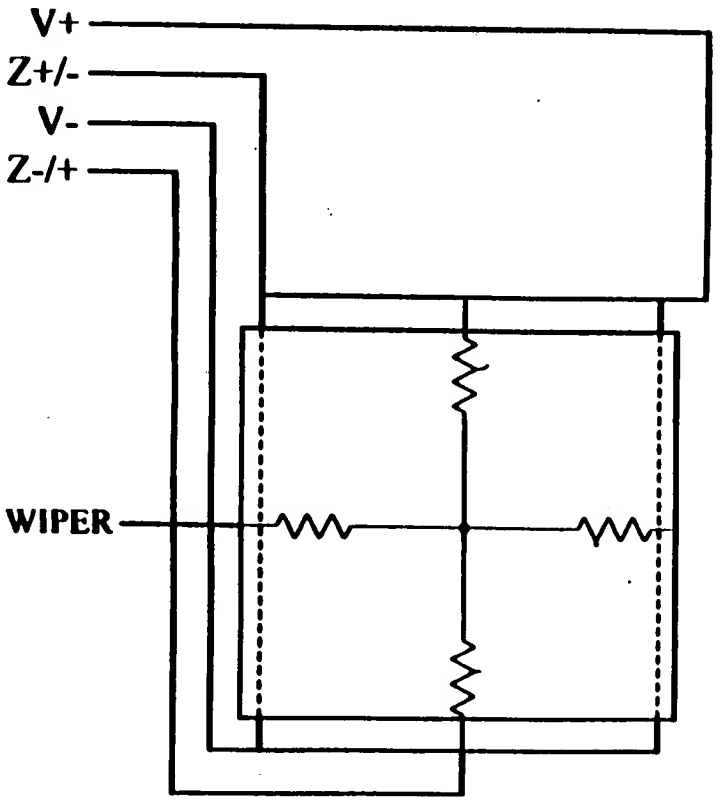


Fig. 6B

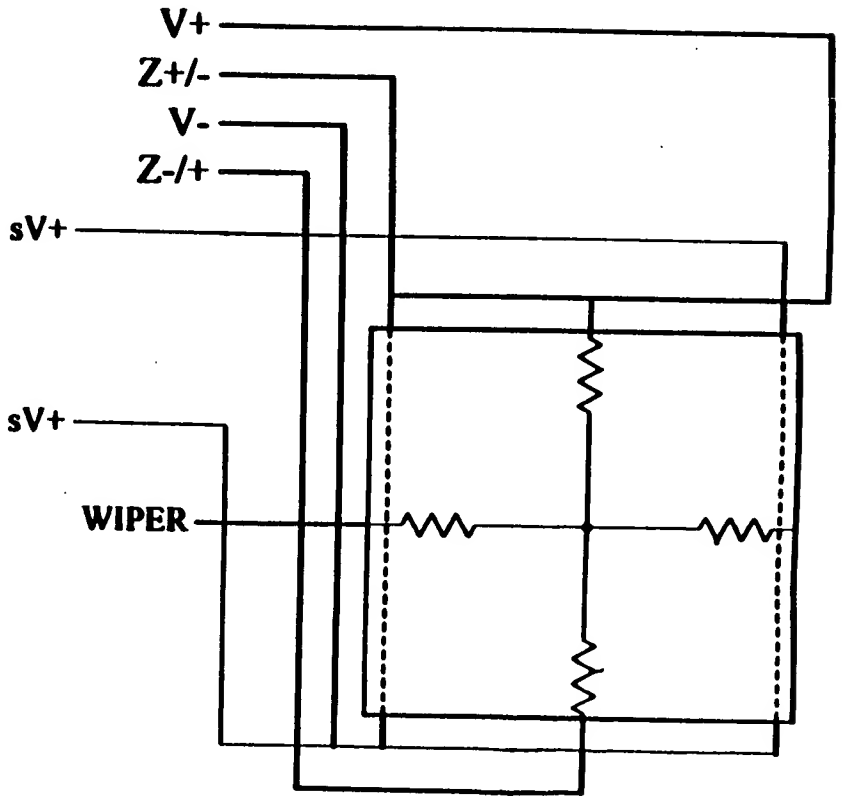
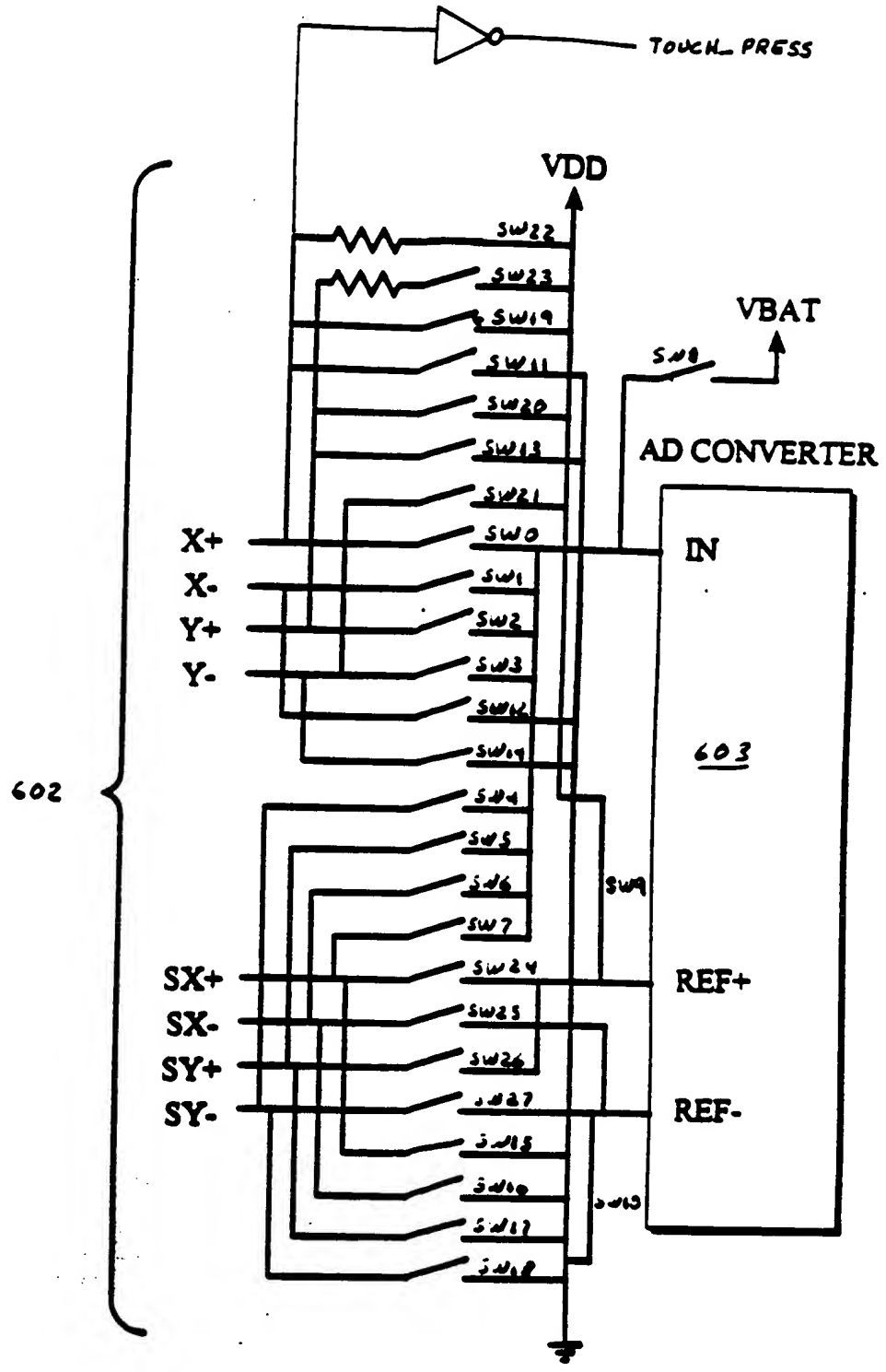


Fig. 6C

d3-2h01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TOUCH_PRESS
VDD
VBAT
SW8
AD CONVERTER
IN
603
602
X+
X-
Y+
Y-
SX+
SX-
SY+
SY-
SW9
SW10
REF+
REF-
SW22
SW23
SW19
SW11
SW20
SW13
SW21
SW0
SW1
SW2
SW3
SW12
SW14
SW4
SW5
SW6
SW7
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SW26
SW27
SW15
SW16
SW17
SW18

Fig. 6E

1042-EP

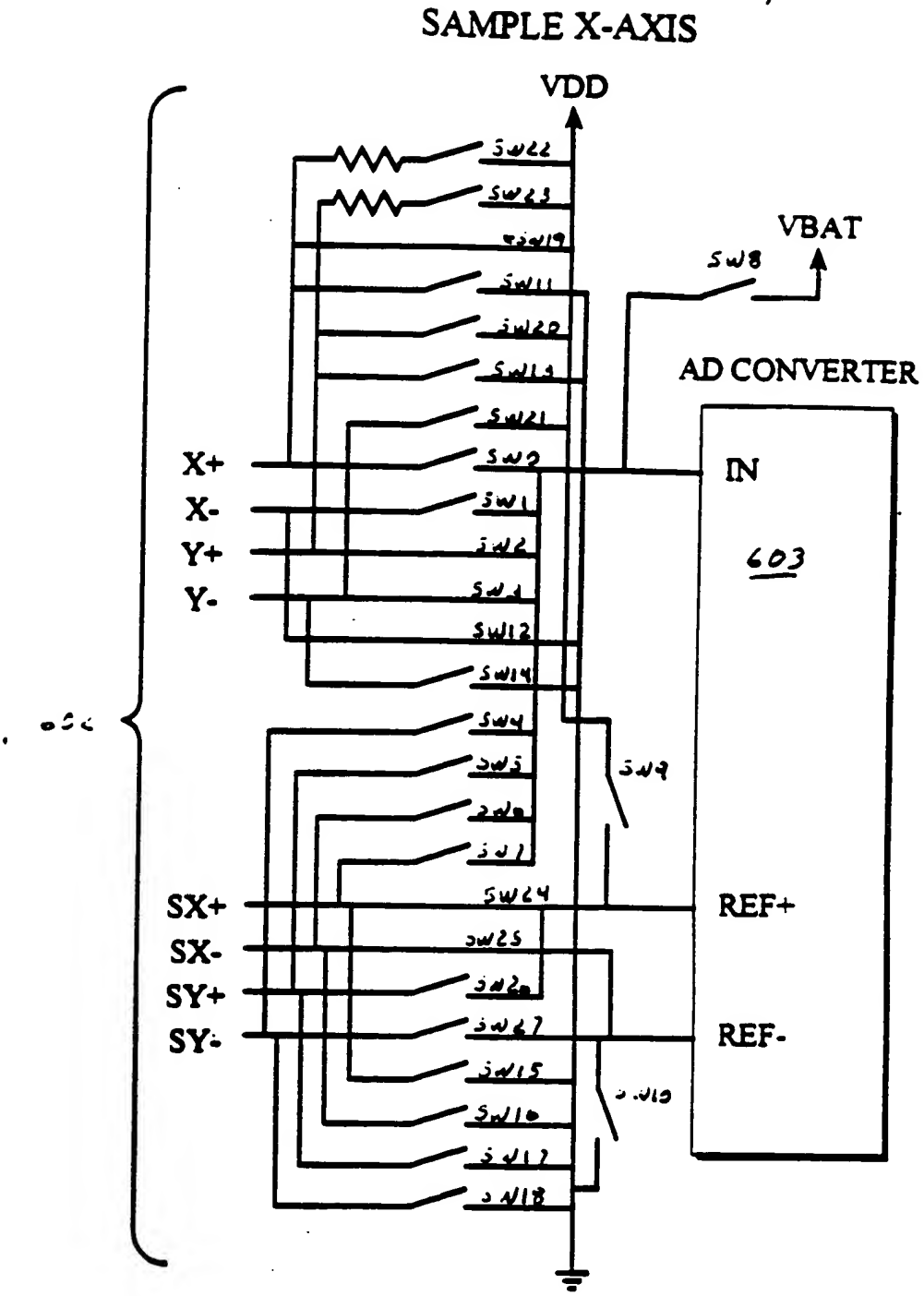

Fig. 6F

1042-EP

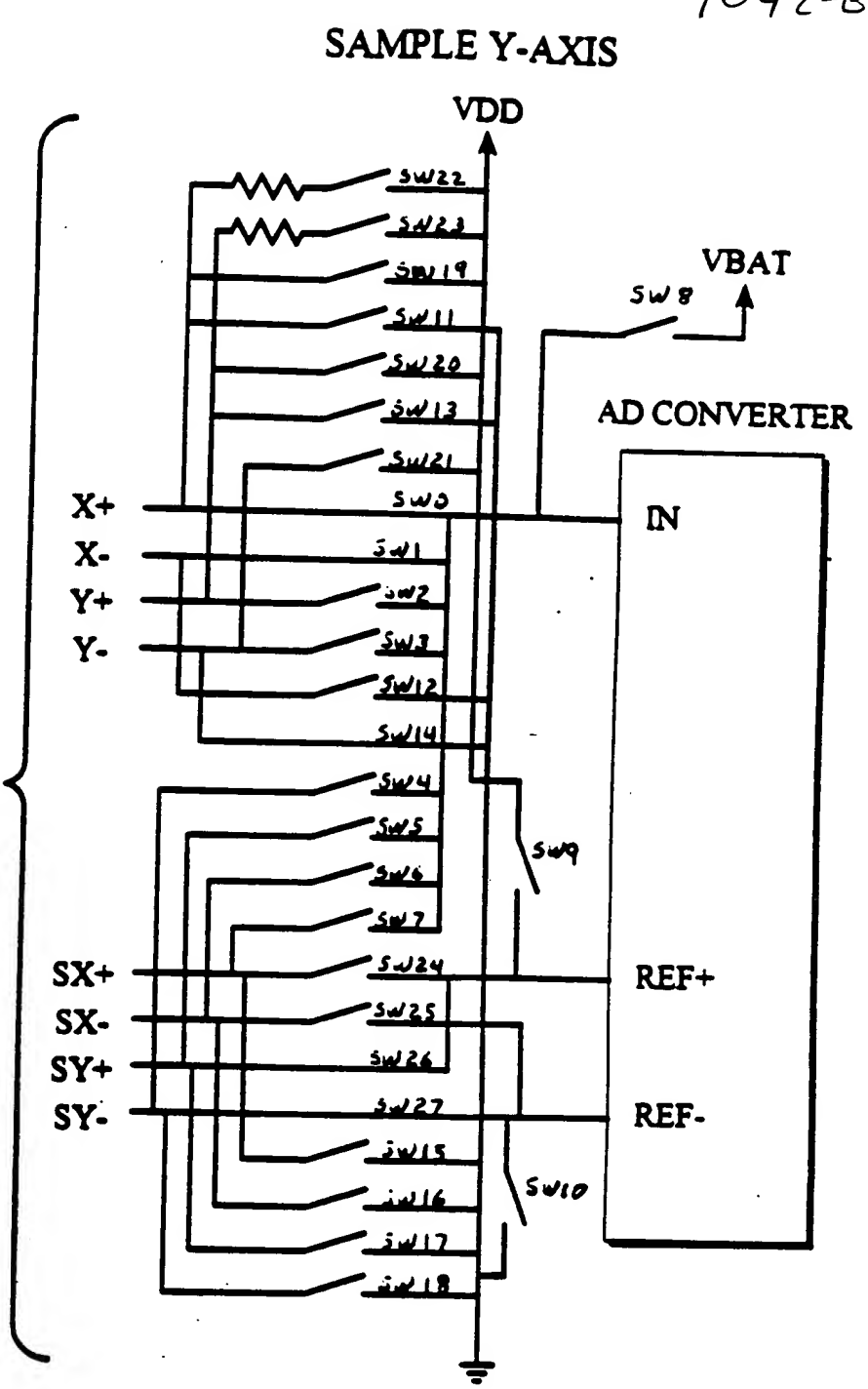

Fig. 6G

1042-EP

DISCHARGE ALL LINES

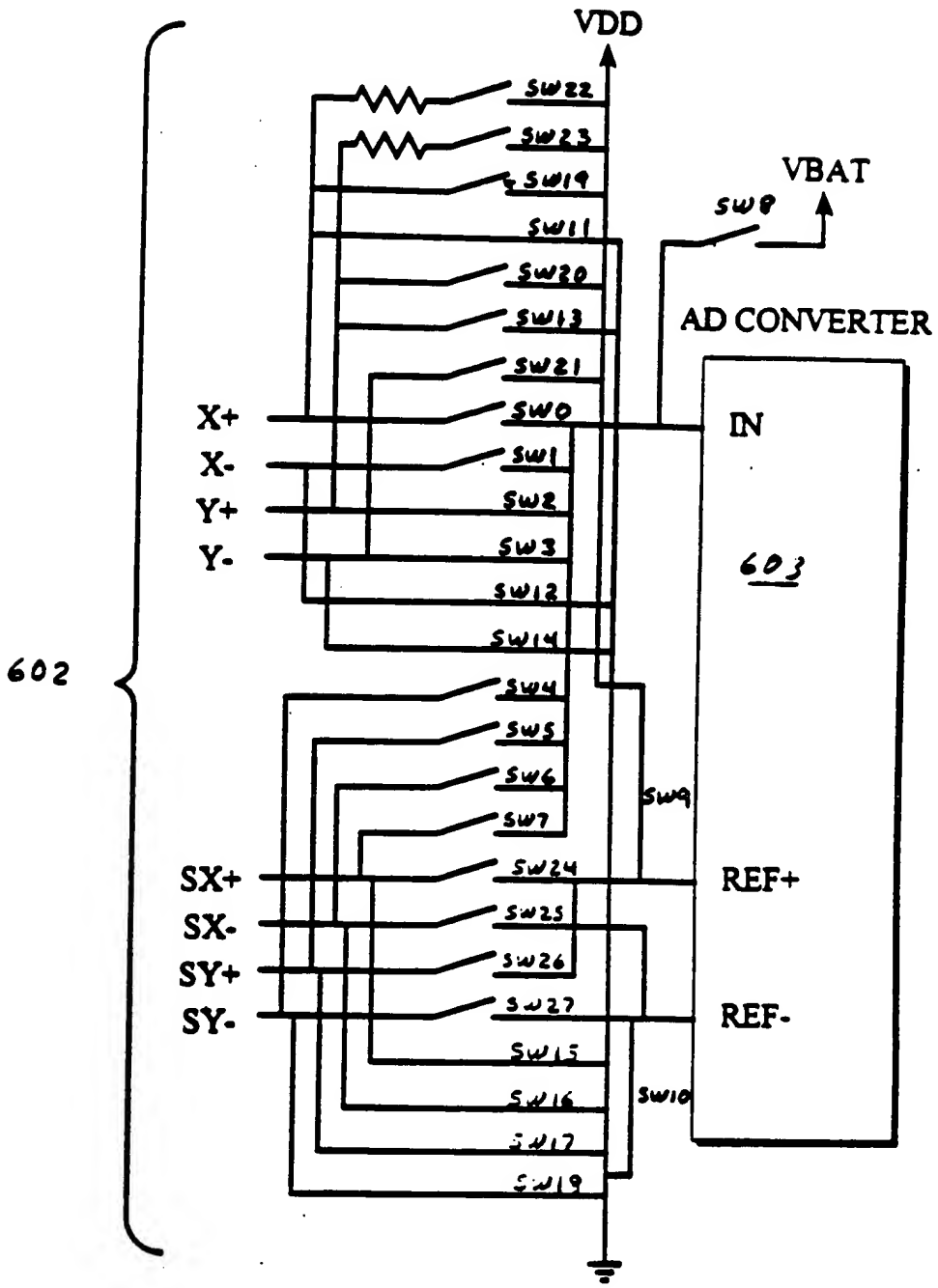

Fig. 6H

1042-EP

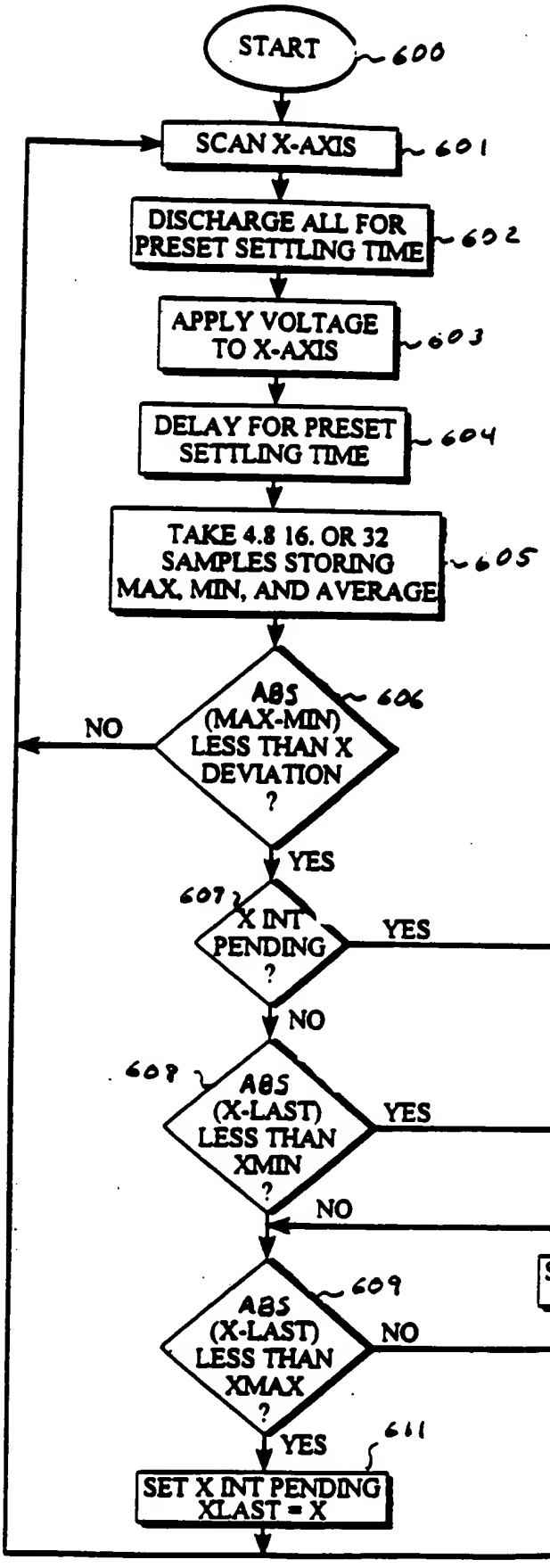

Fig. 6I
Sheet 1

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1042-EP

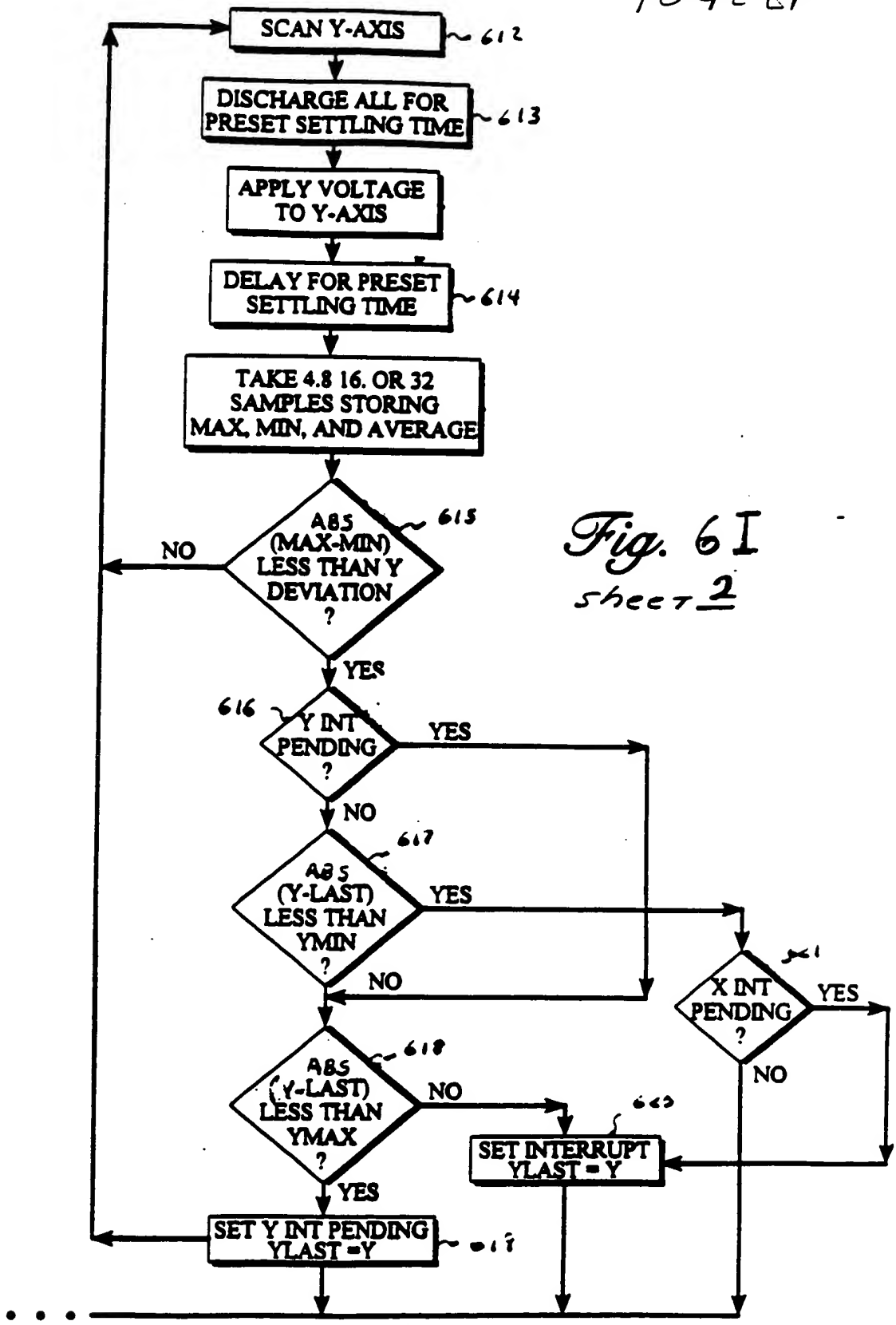


Fig. 6I
sheet 2

1042-EP 3

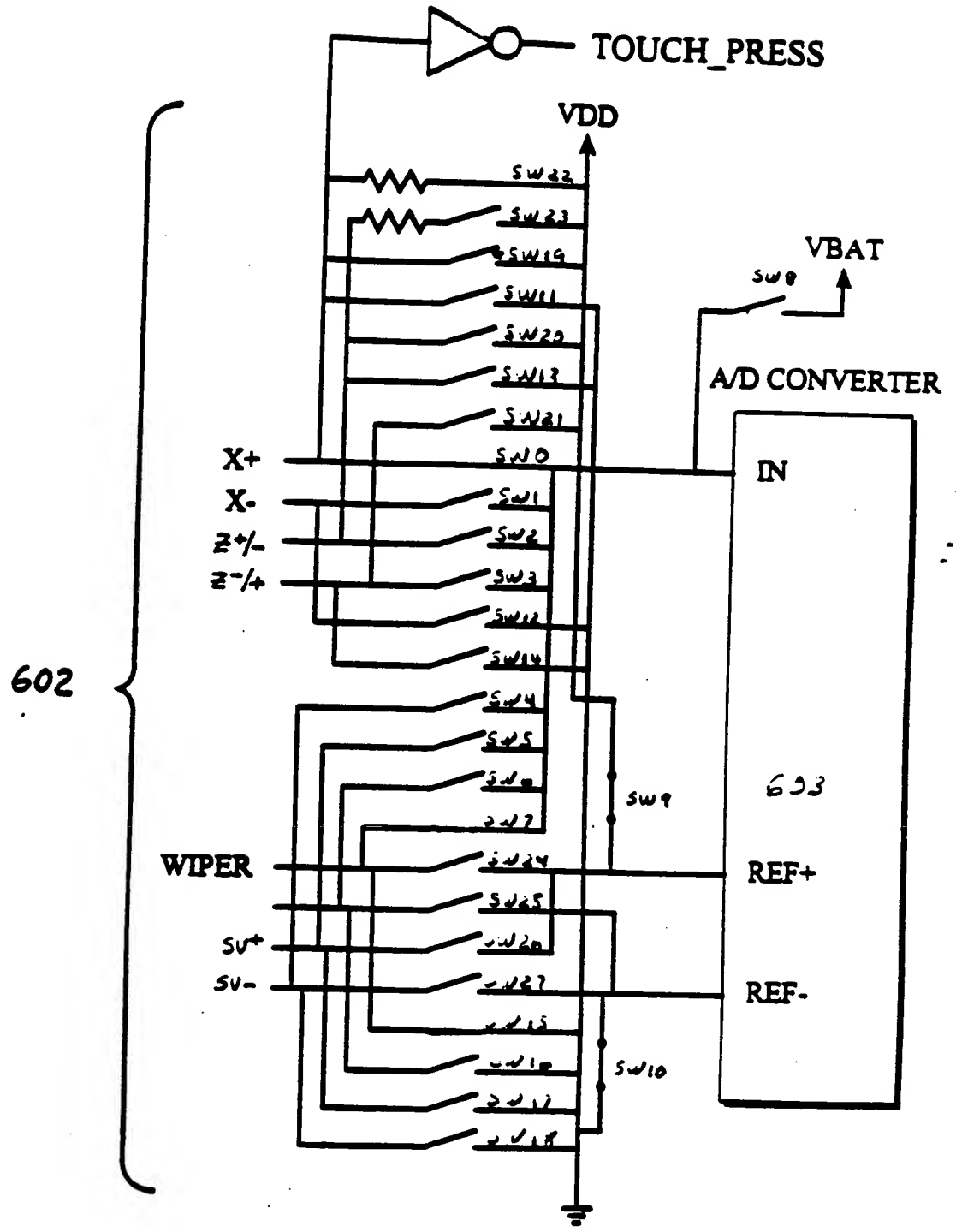


Fig. 6J

1042-EP

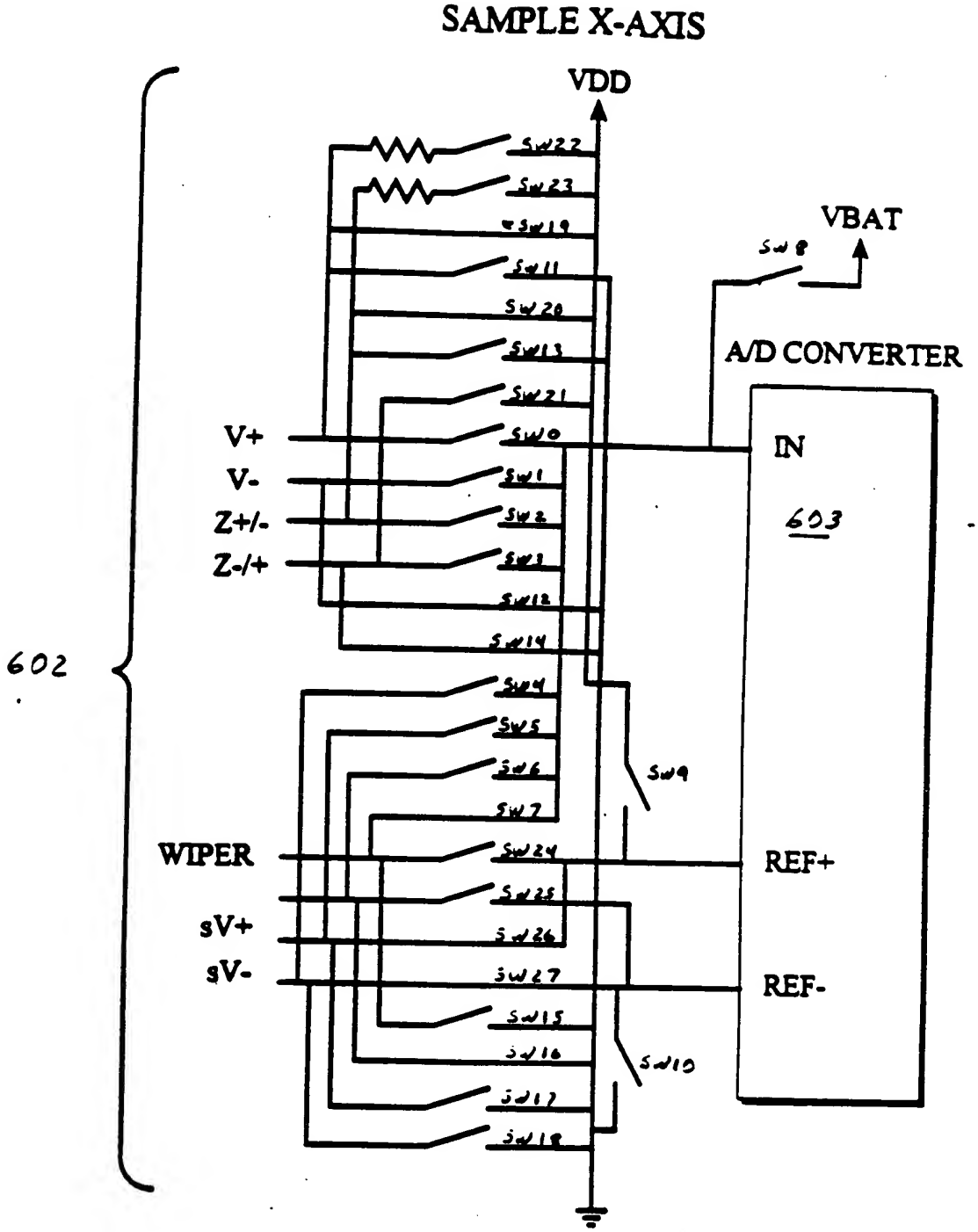


Fig. 6K

1042-EP

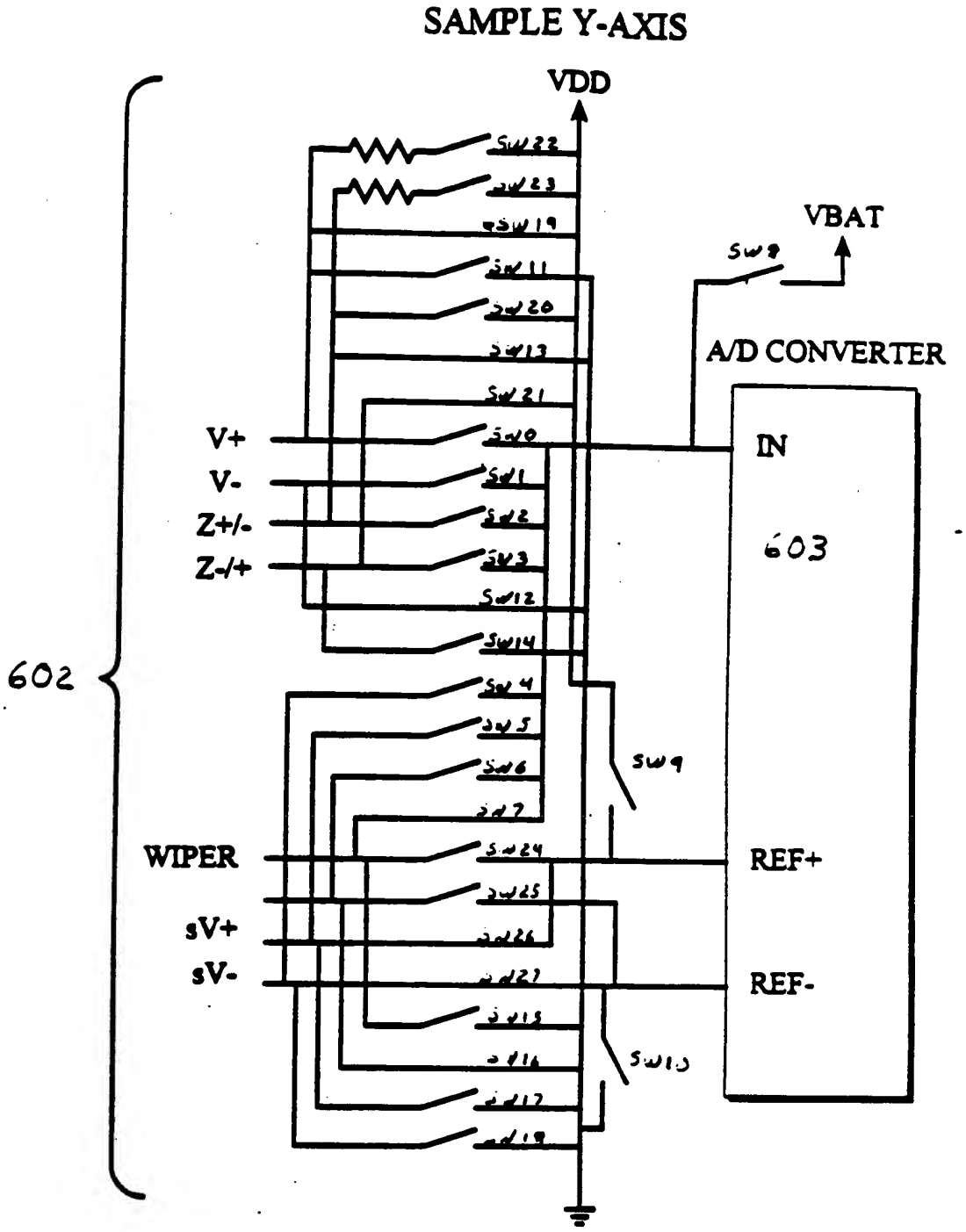


Fig. 6L

1042-EP

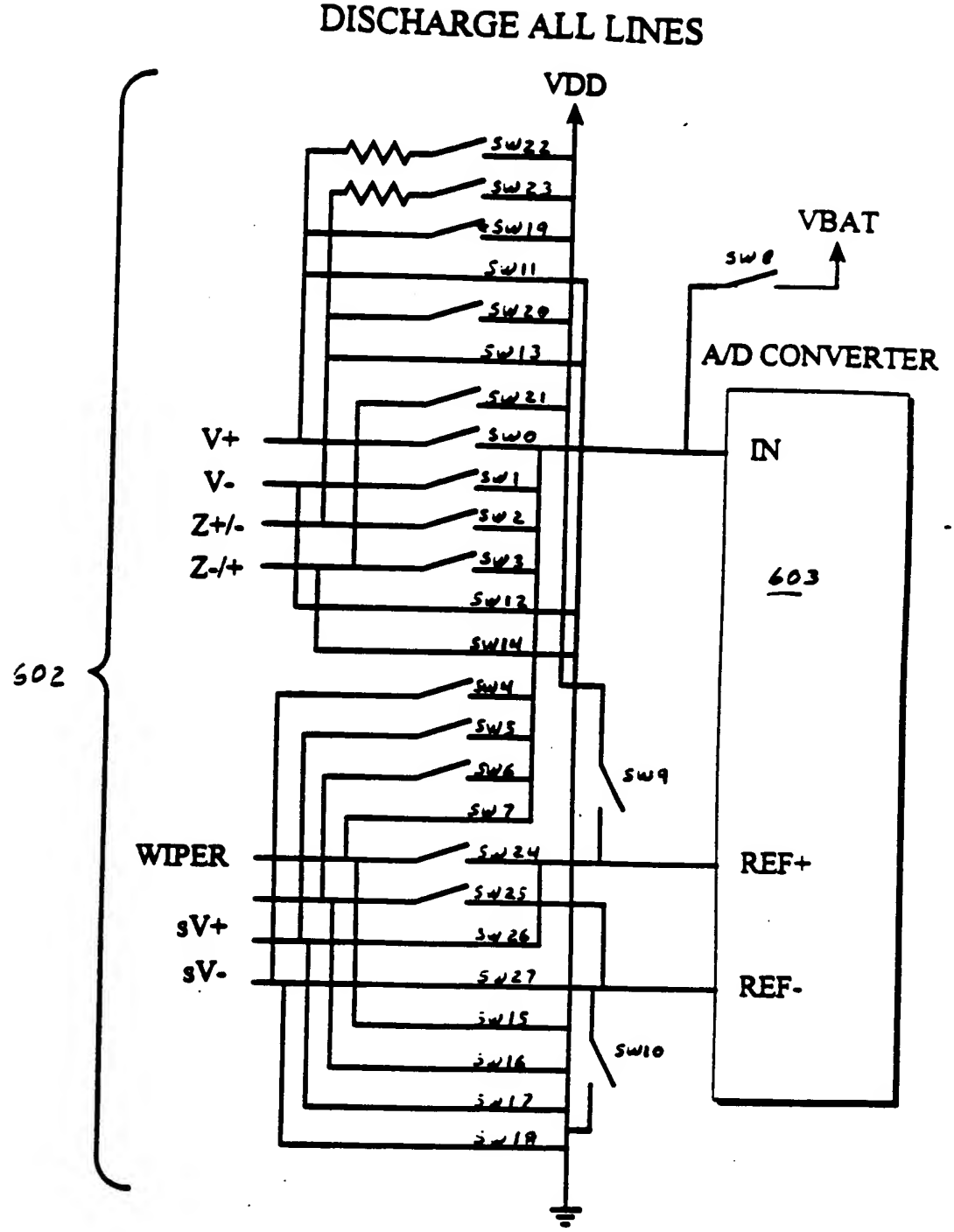
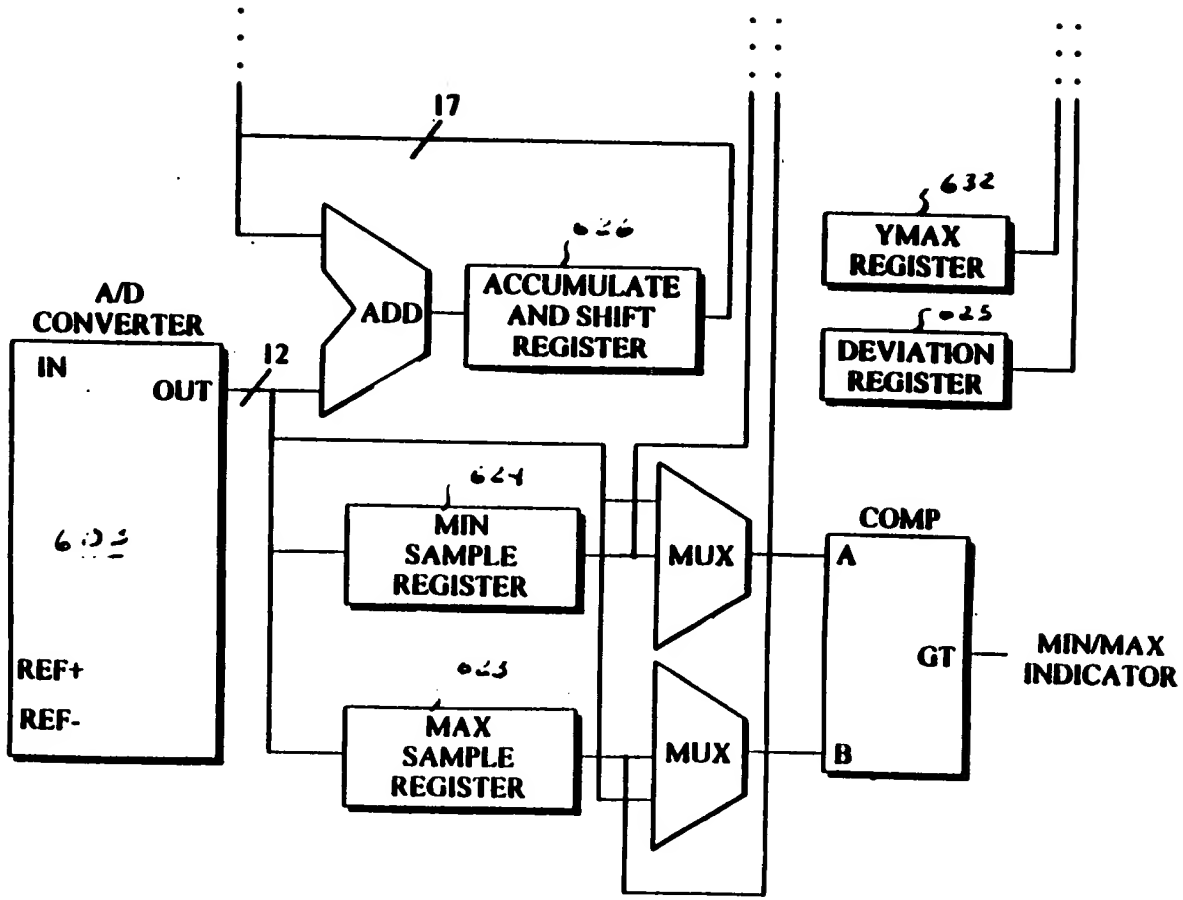


Fig. 6M

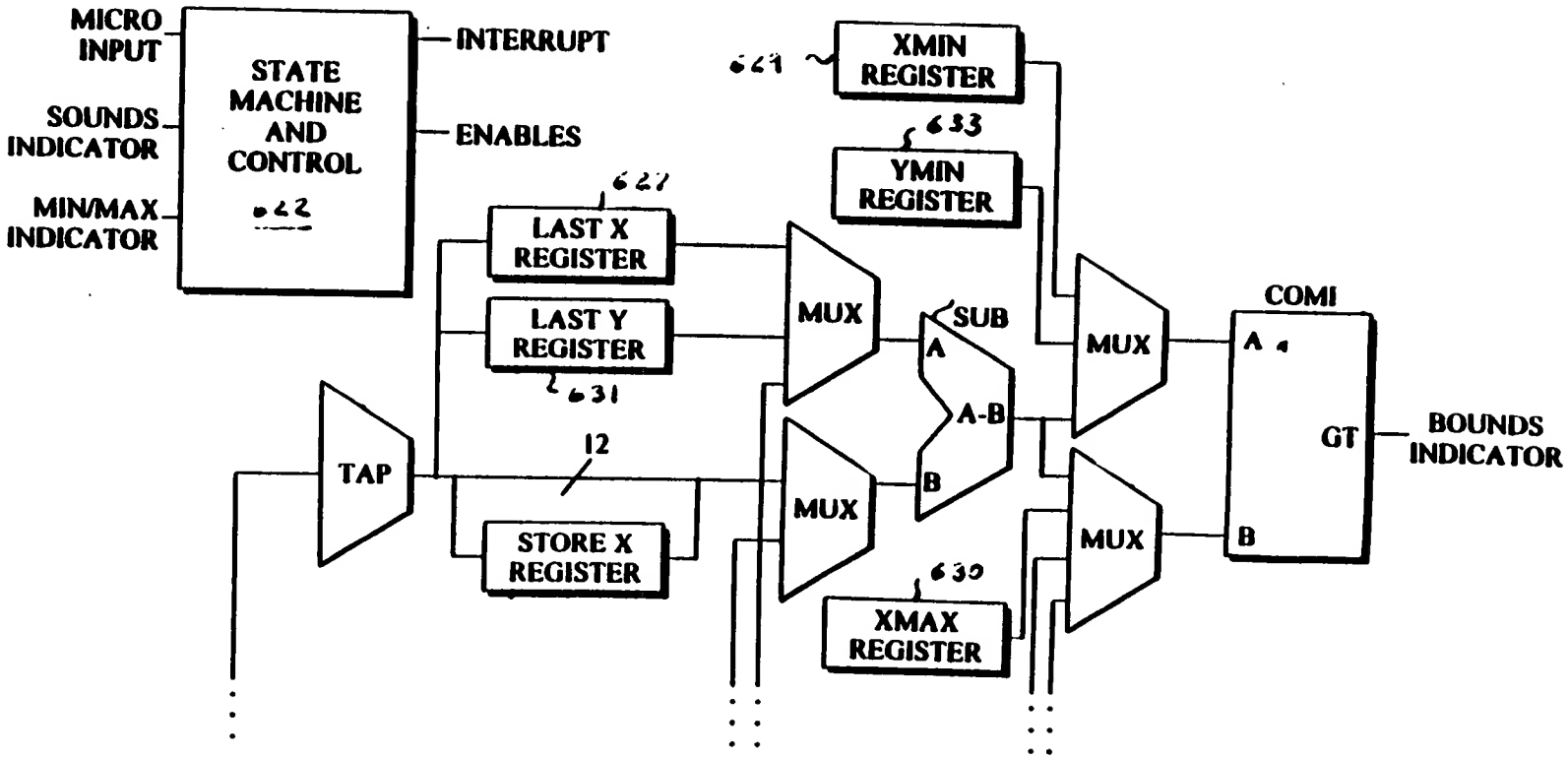
006090 6597 6960



Sheet 2 Fig. 6N

10,427,201

006090 6597 6560



Sheet 1

Fig. 6N.

93-2401

5 wire detect press

1042-EP

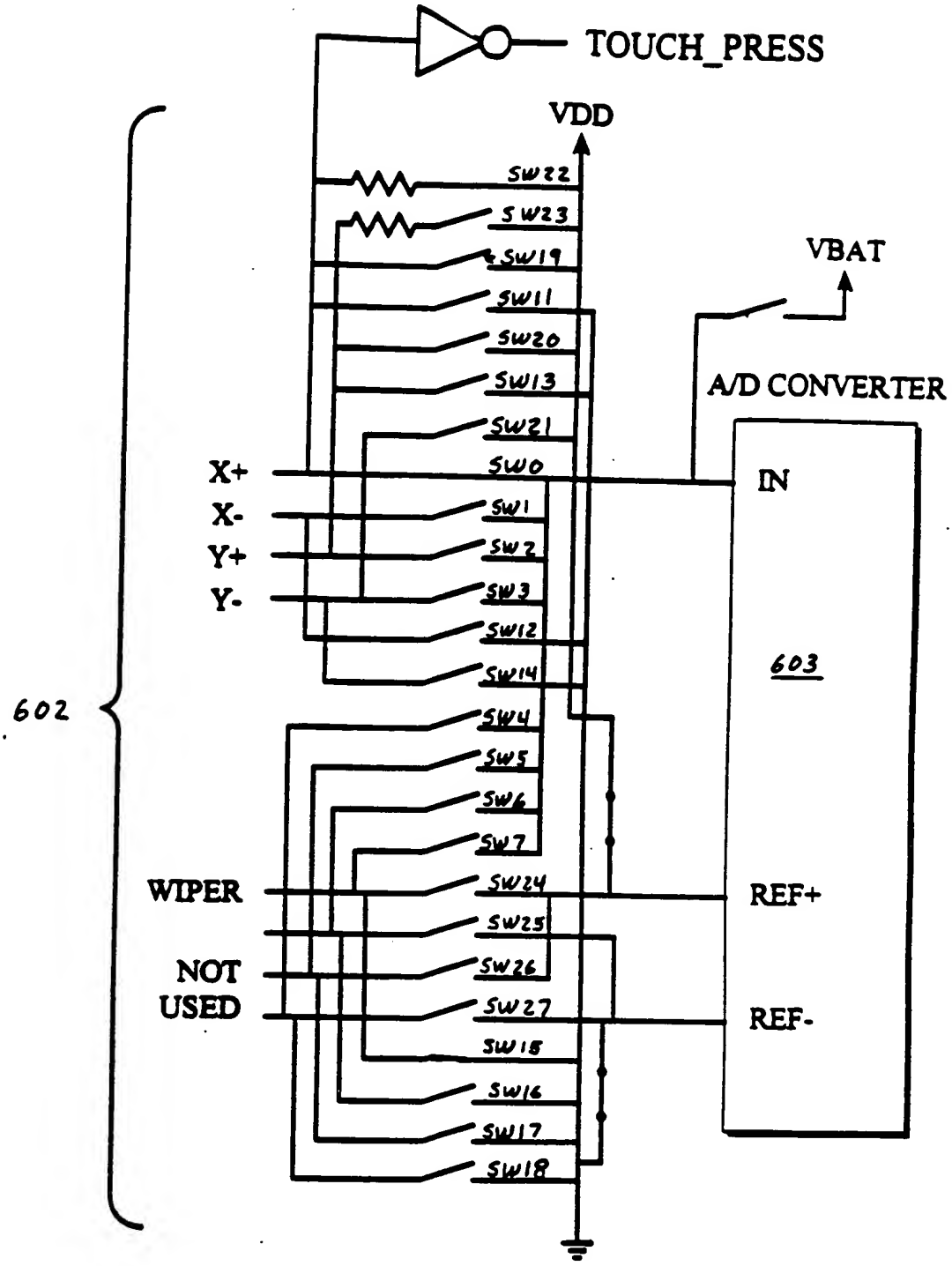


Fig. 6Q

1042-EP

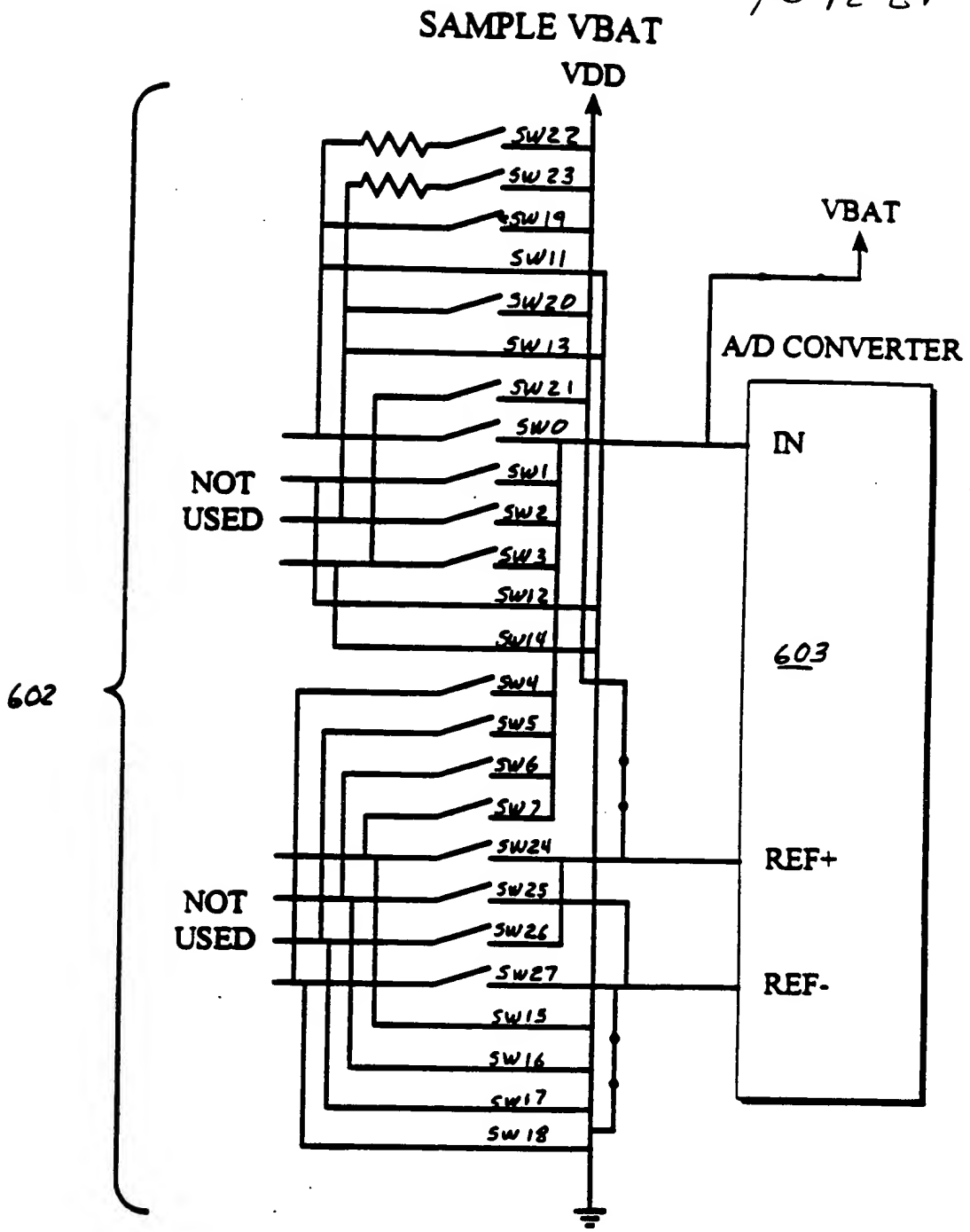


Fig. 6P

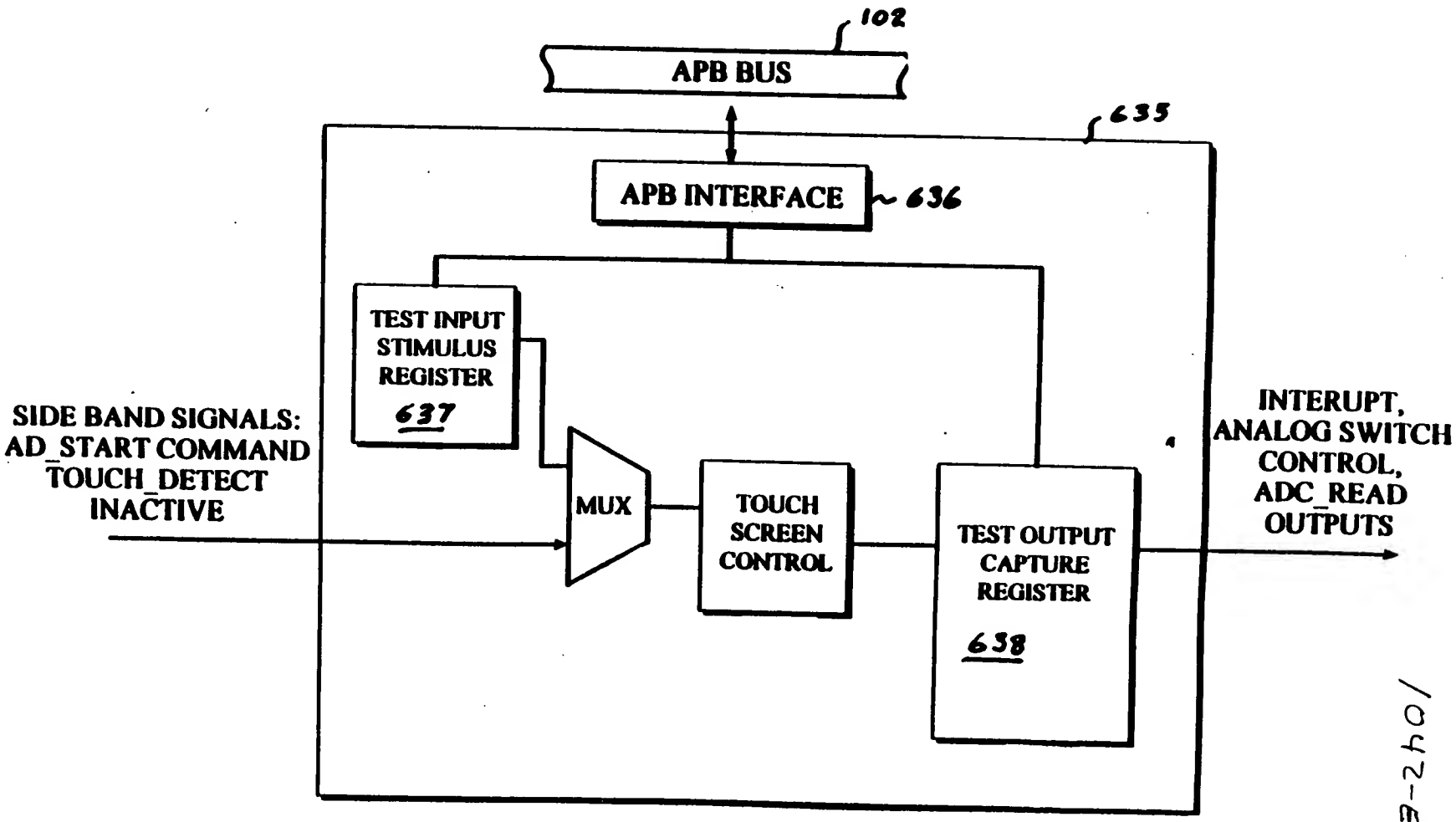
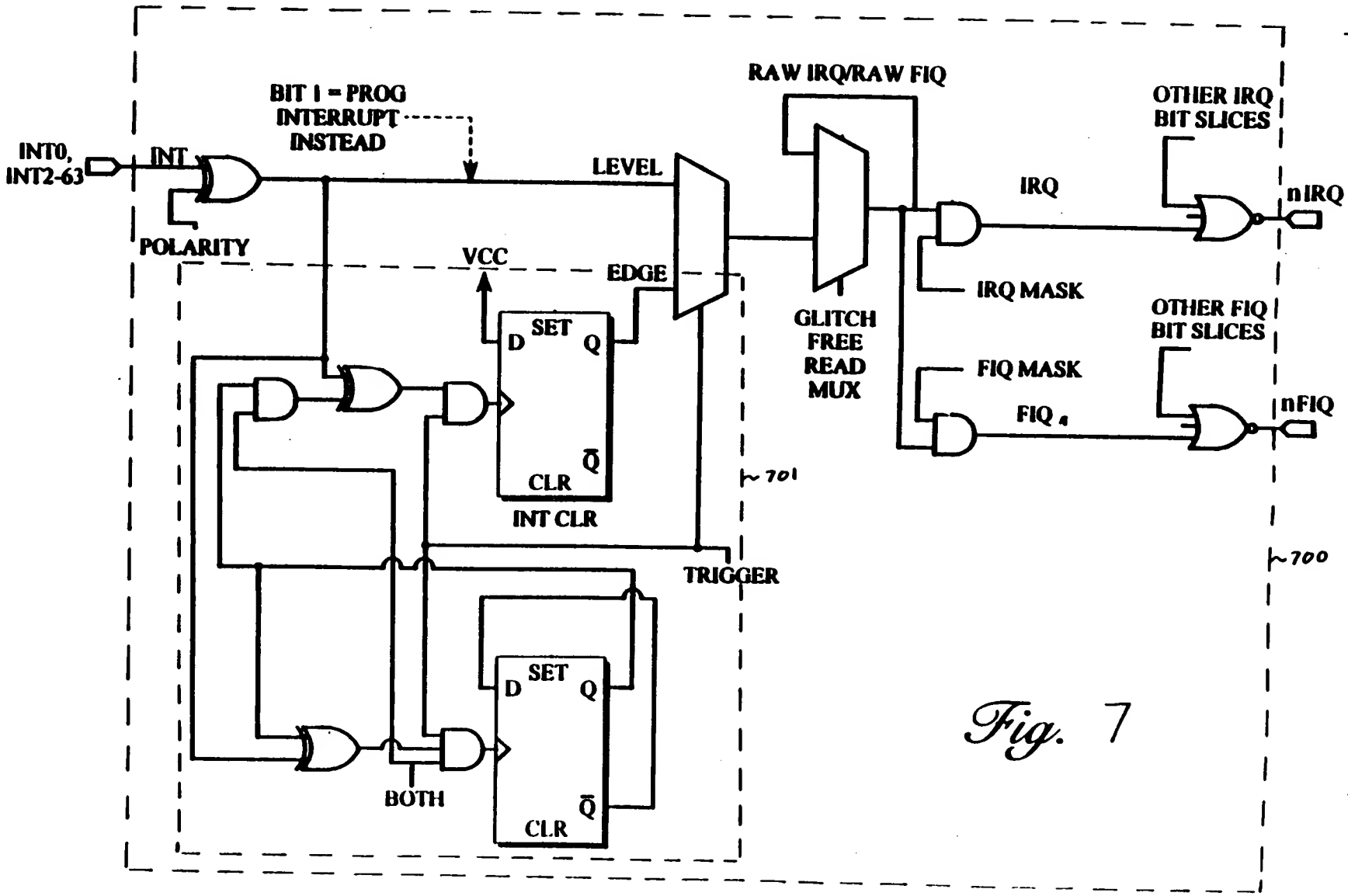


Fig. 6Q

03-2401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INT2-63
INT
POLARITY
BIT 1 = PROG
INTERRUPT
INSTEAD
LEVEL
EDGE
VCC
SET
D
Q
CLR
Q̄
INT CLR
701
TRIGGER
BOTH
RAW IRQ/RAW FIQ
GLITCH
FREE
READ
MUX
IRQ
IRQ MASK
FIQ MASK
FIQ
OTHER IRQ
BIT SLICES
nIRQ
OTHER FIQ
BIT SLICES
nFIQ
700

Fig. 7

03-2401

0060956 6556560

1042-EP

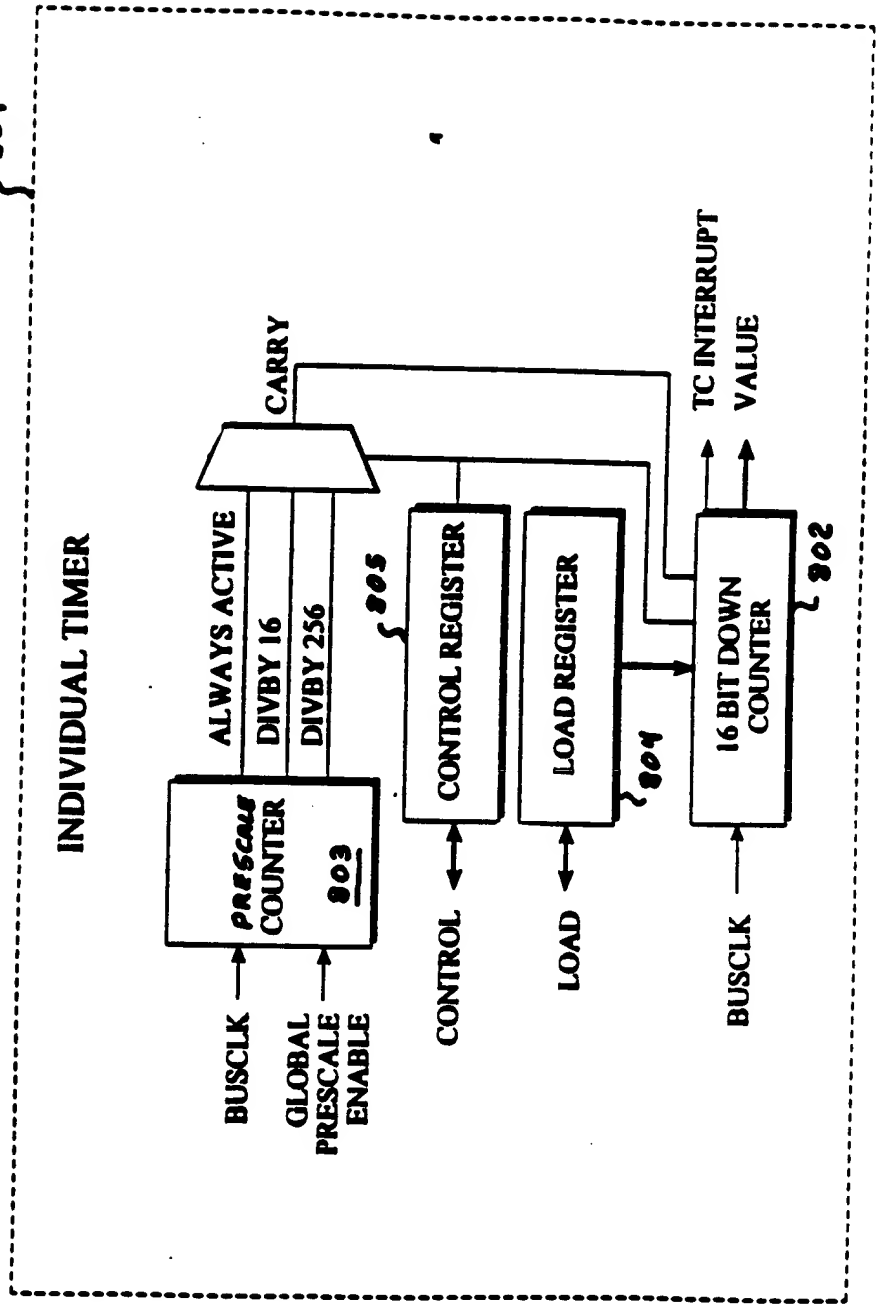


Fig. 8A

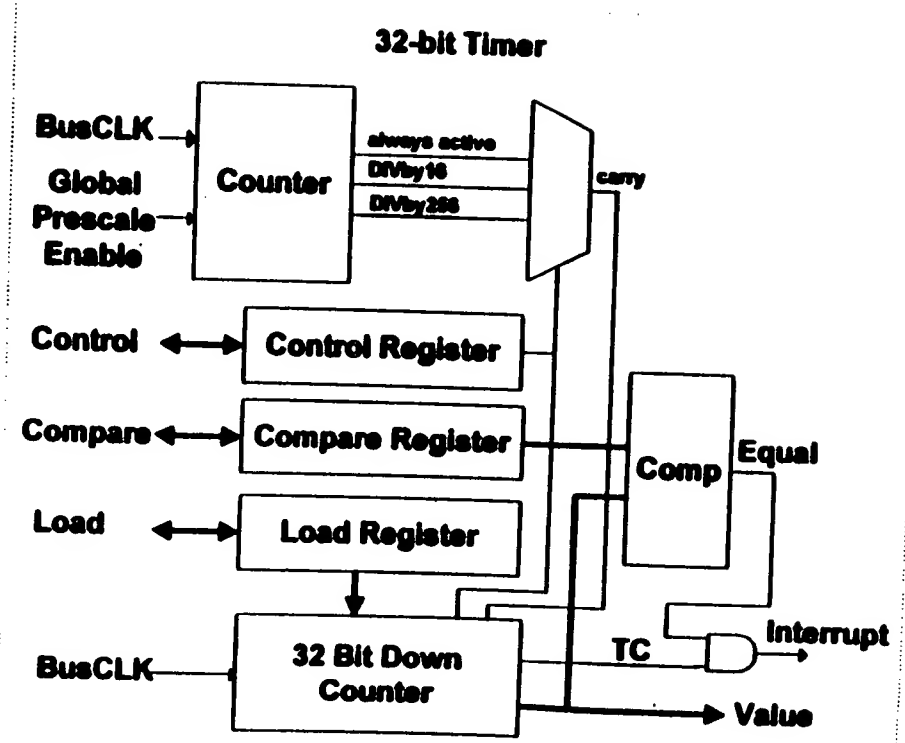


FIG. 8B

1042-EP

1042-EP

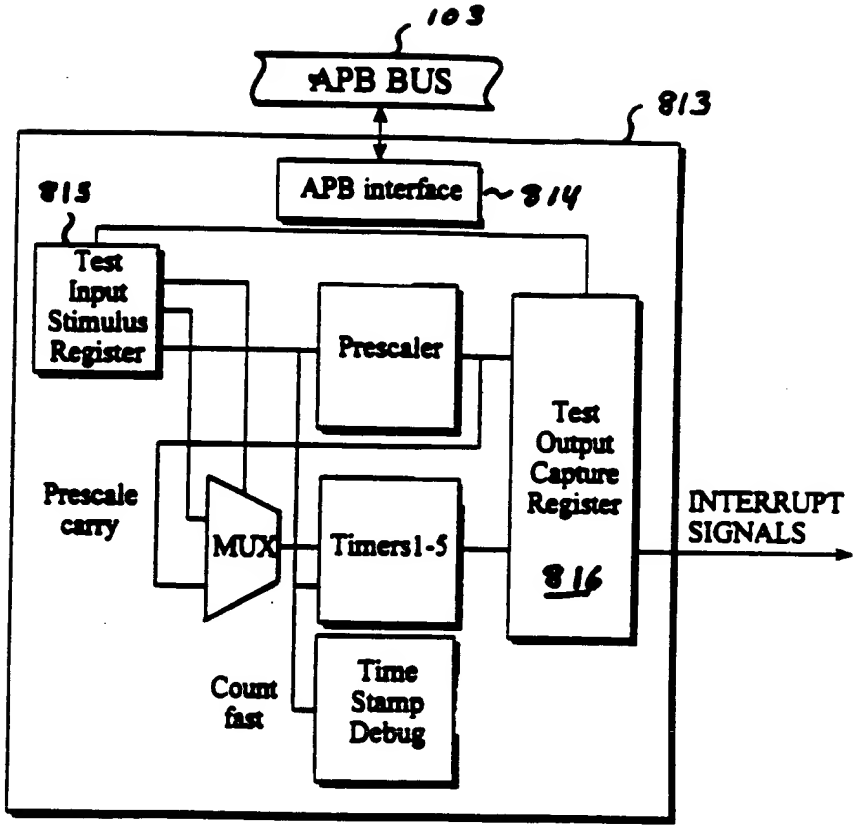


Fig. 8C

006050 "6597"6560

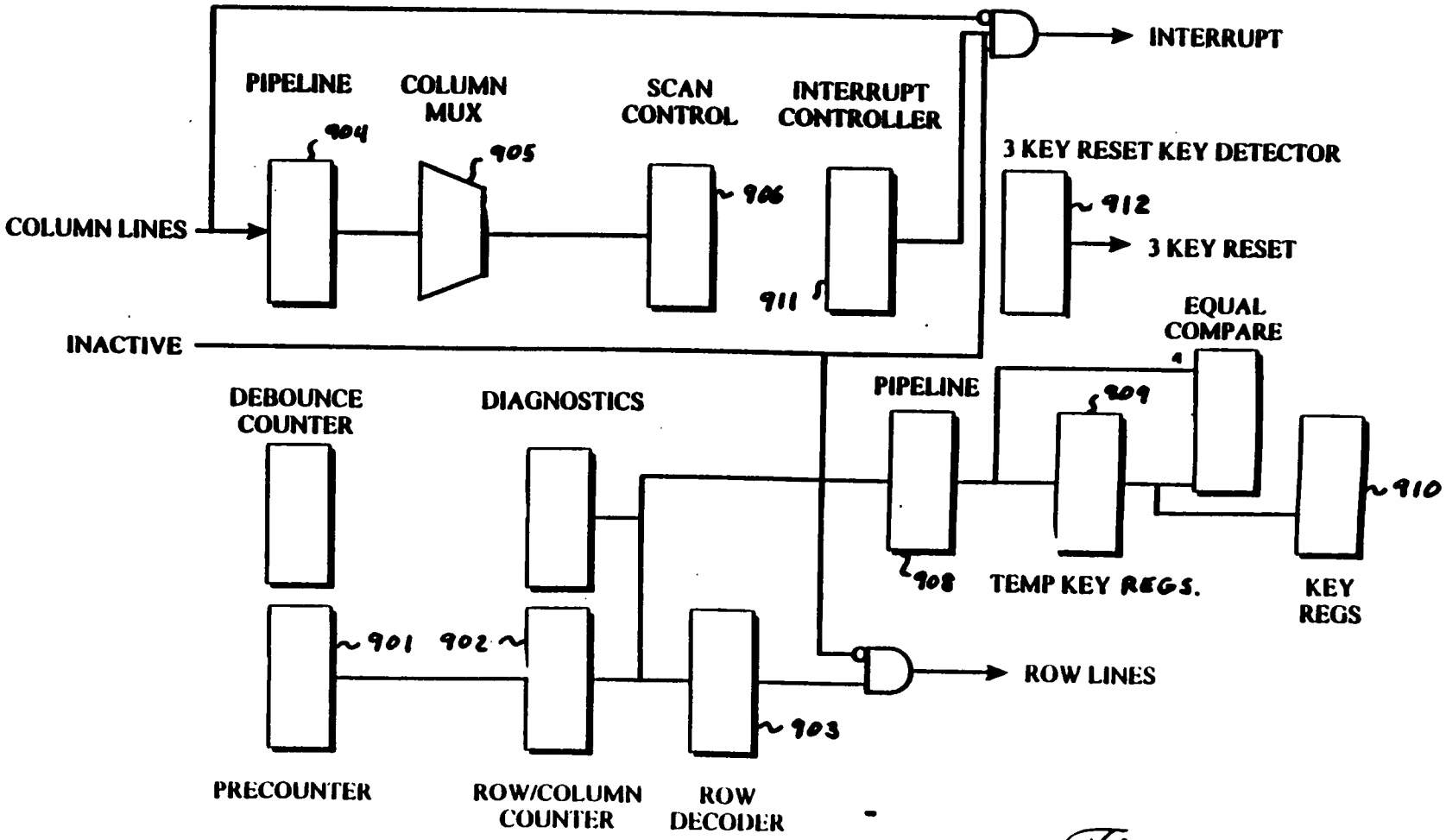


Fig. 9A

042-EP

006090 6597 6560

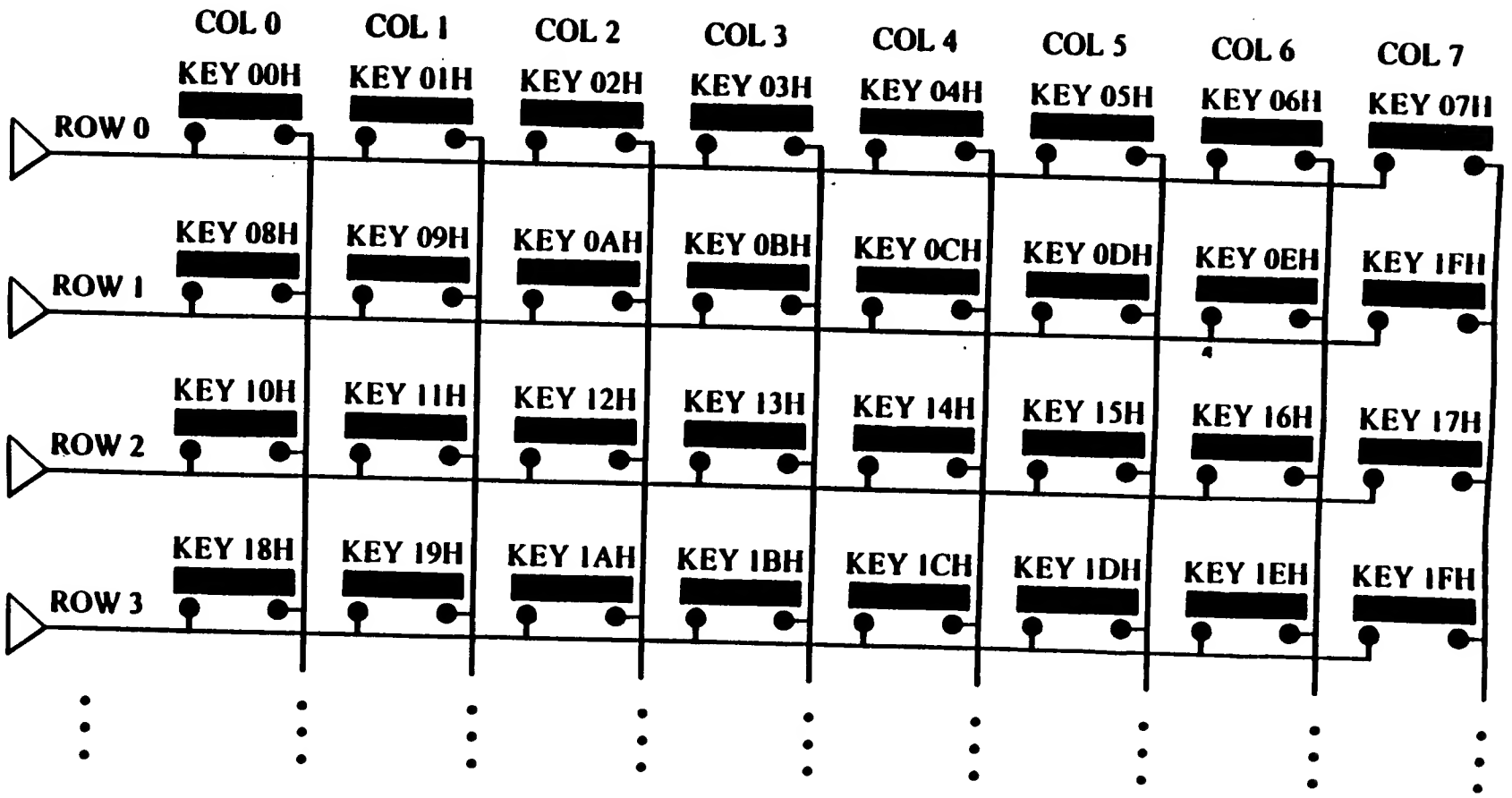
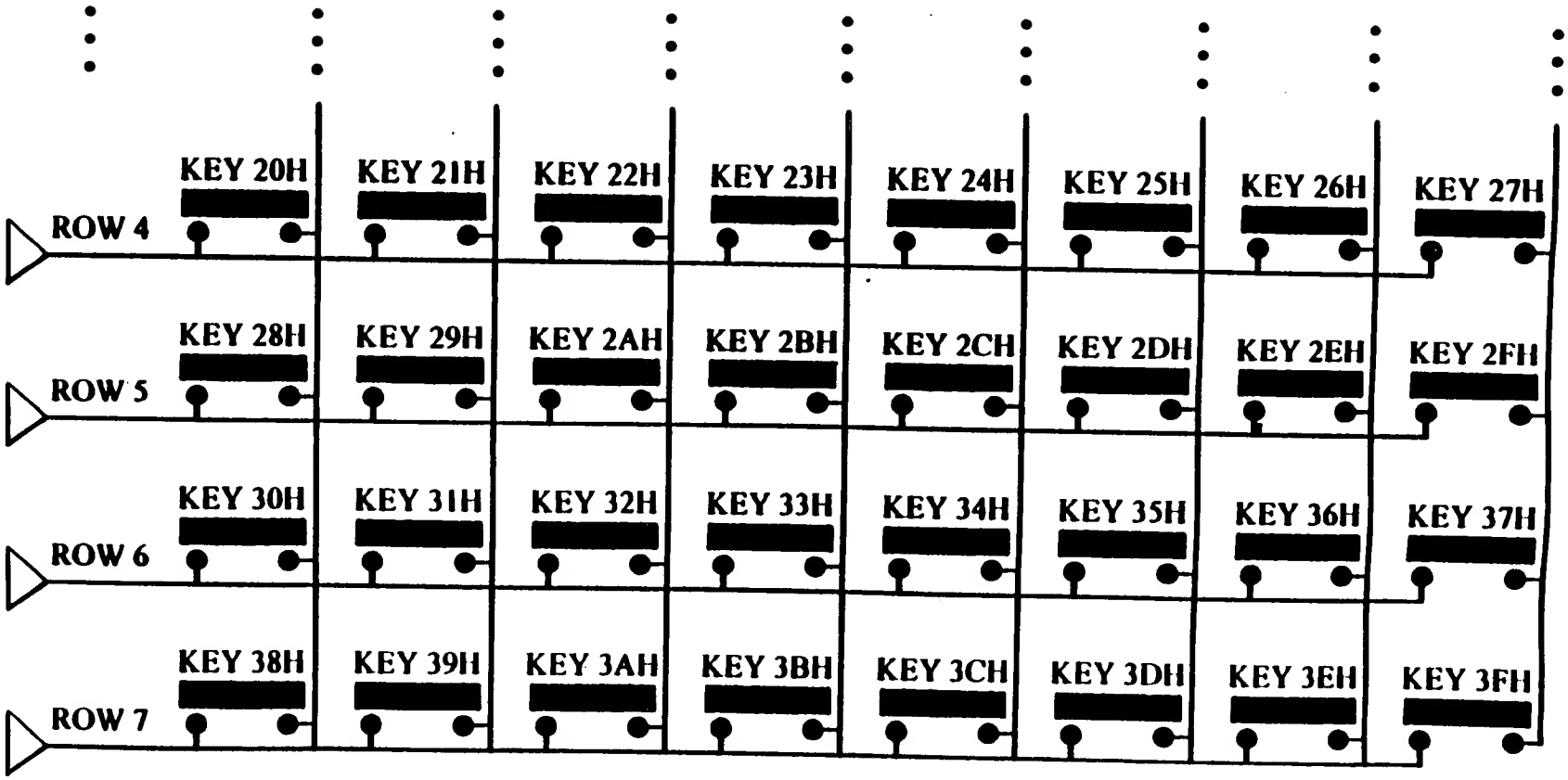


Fig. 9B

(sheet 1)

09/2-EP

000090 6976560



8x8 KEY ARRAY

dg-2401

Fig. 9B
(sheet 2)

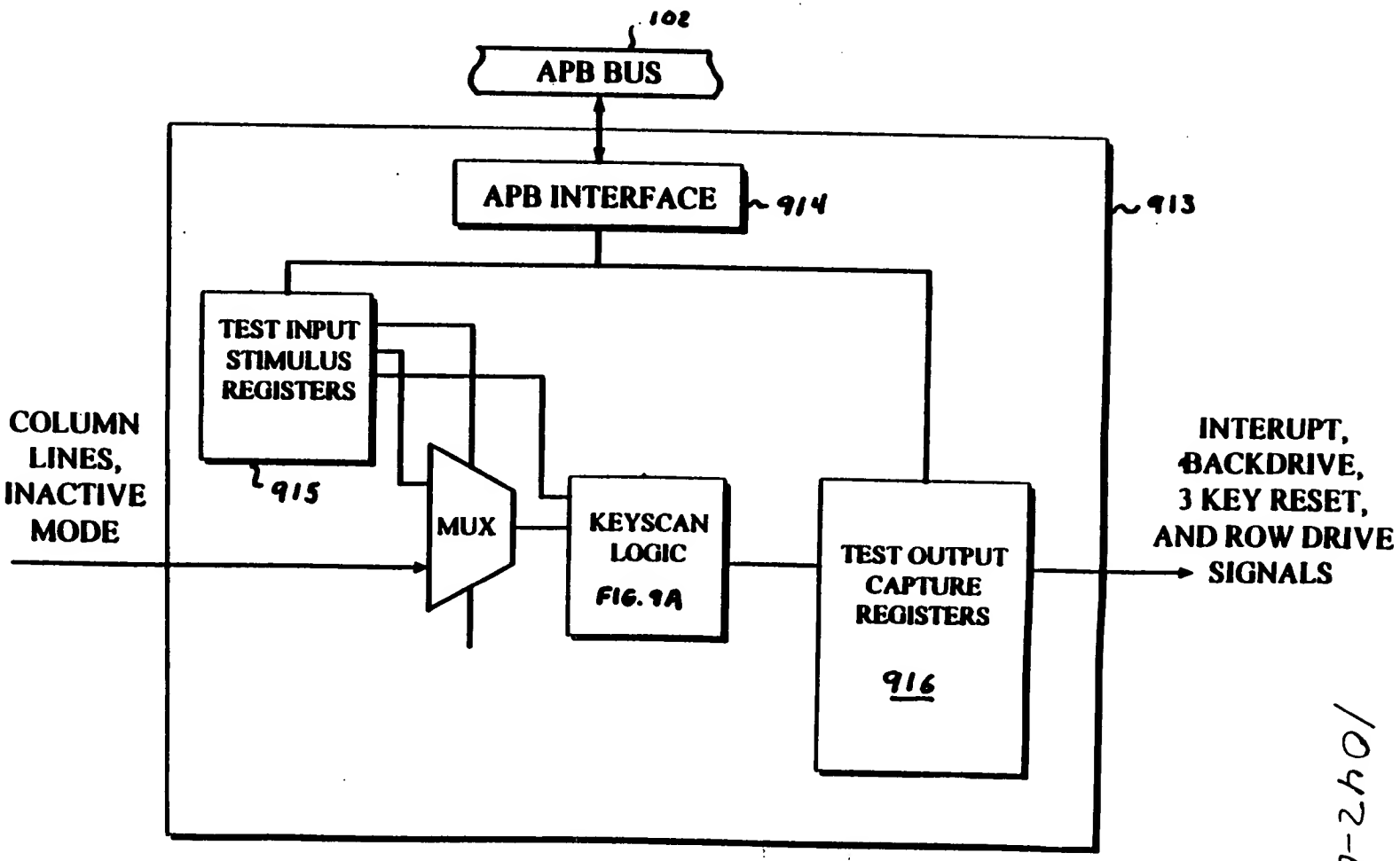

102
APB BUS
APB INTERFACE
914
913
TEST INPUT STIMULUS REGISTERS
915
COLUMN LINES, INACTIVE MODE
MUX
KEYSCAN LOGIC
FIG. 9A
TEST OUTPUT CAPTURE REGISTERS
916
INTERUPT, BACKDRIVE, 3 KEY RESET, AND ROW DRIVE SIGNALS

Fig. 9C

006090 6597 6560

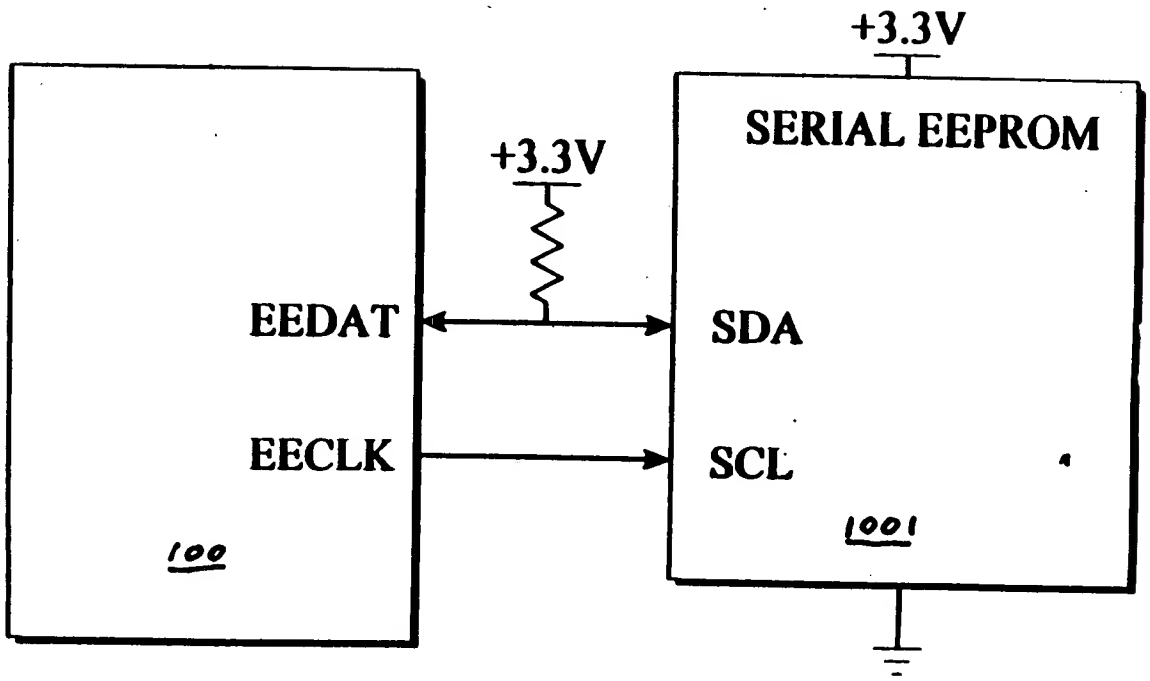


Fig. 10A

04-2701

006090 6597659

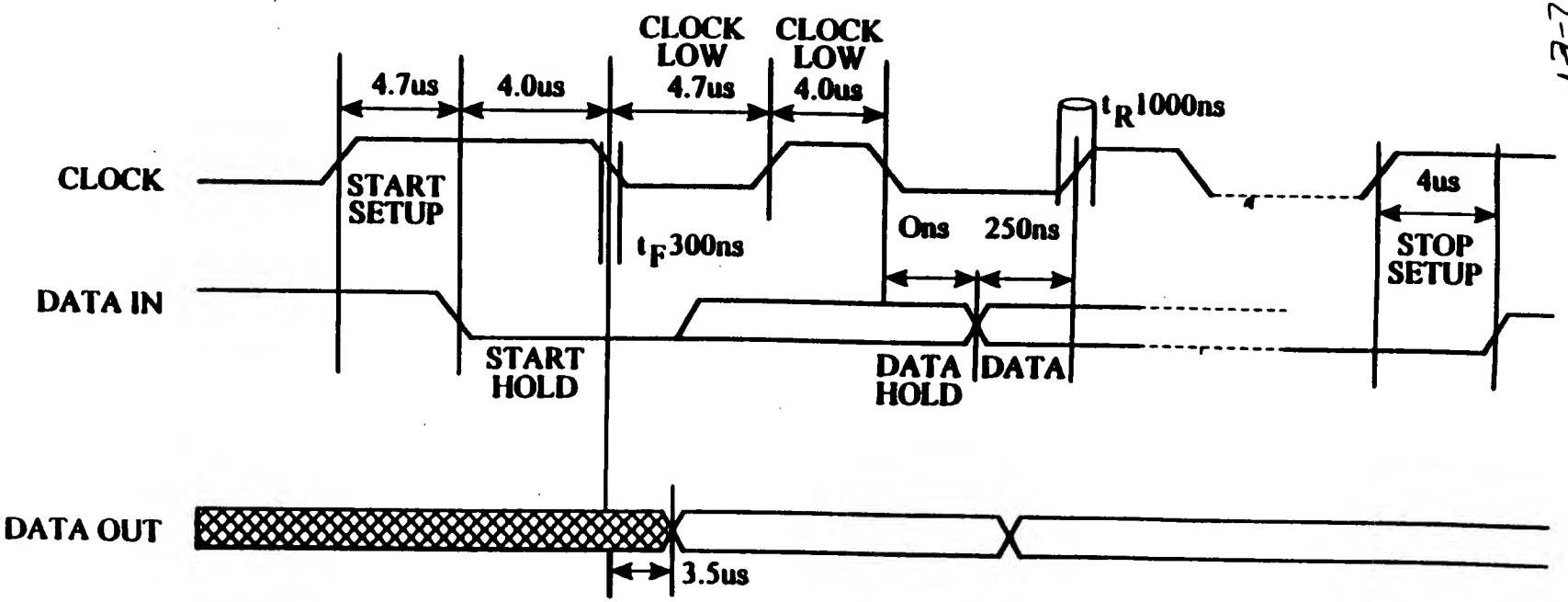


Fig. 10B

DE-2401

006090 "0597"6560

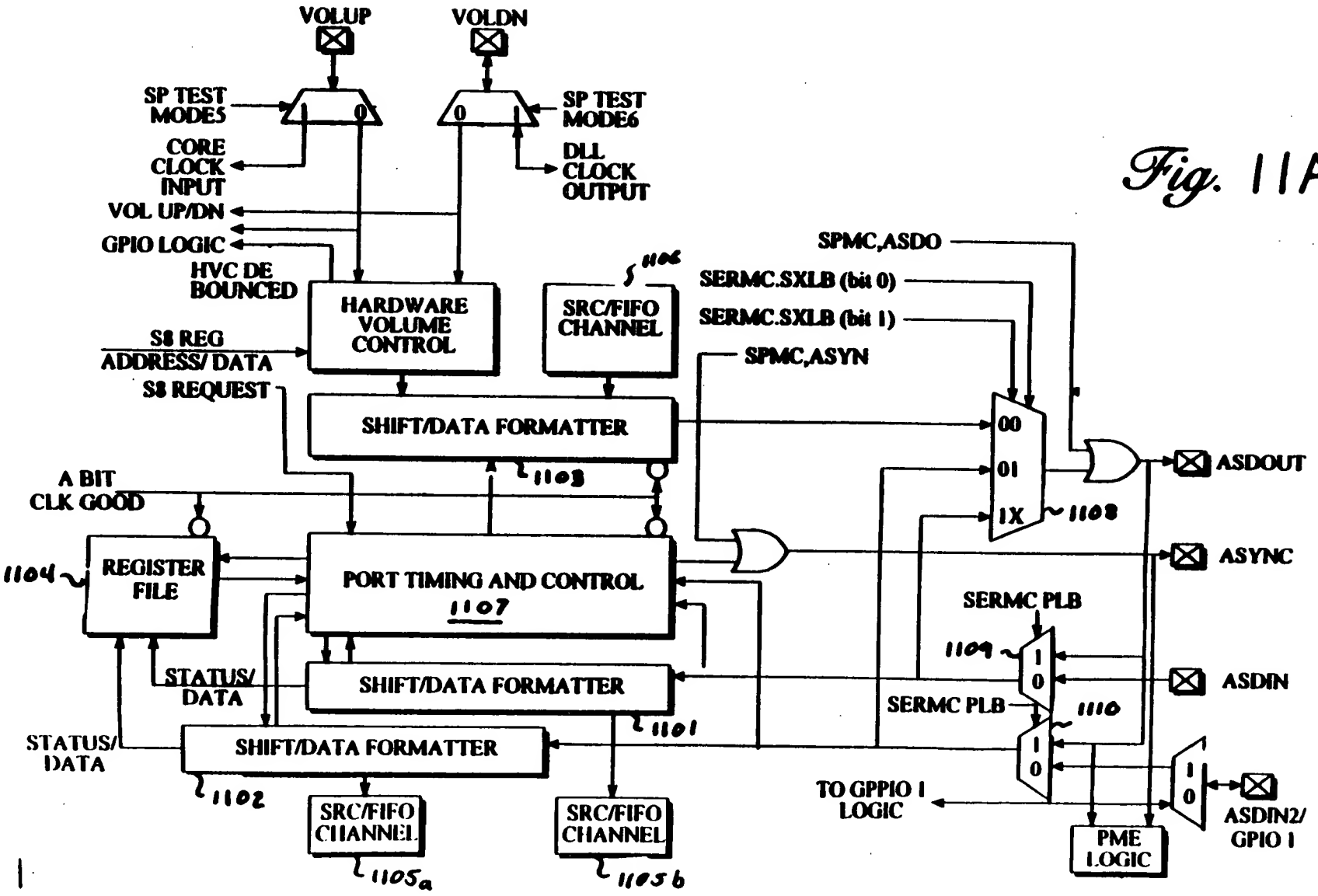


Fig. 11A

09/27-69

006090 "9991G960

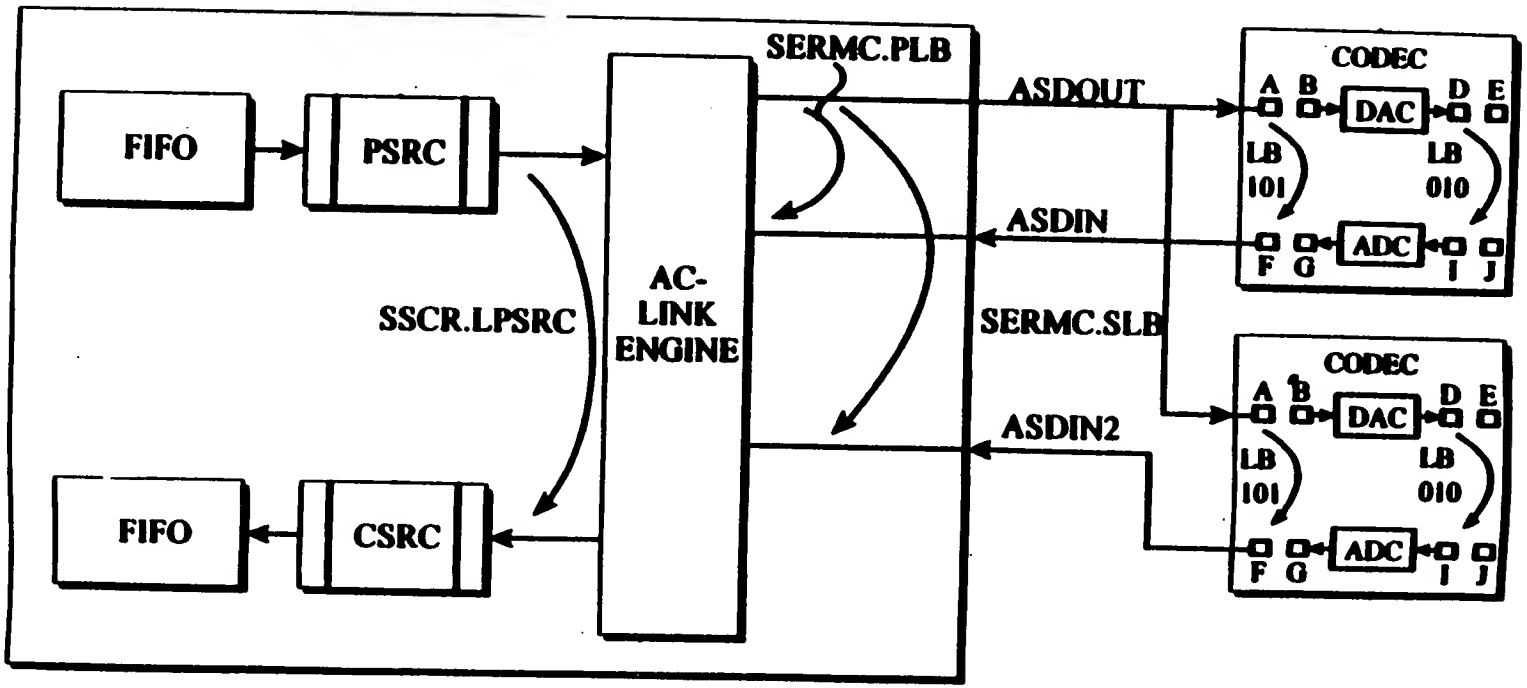


Fig. 11B

03-2401

0060902591650

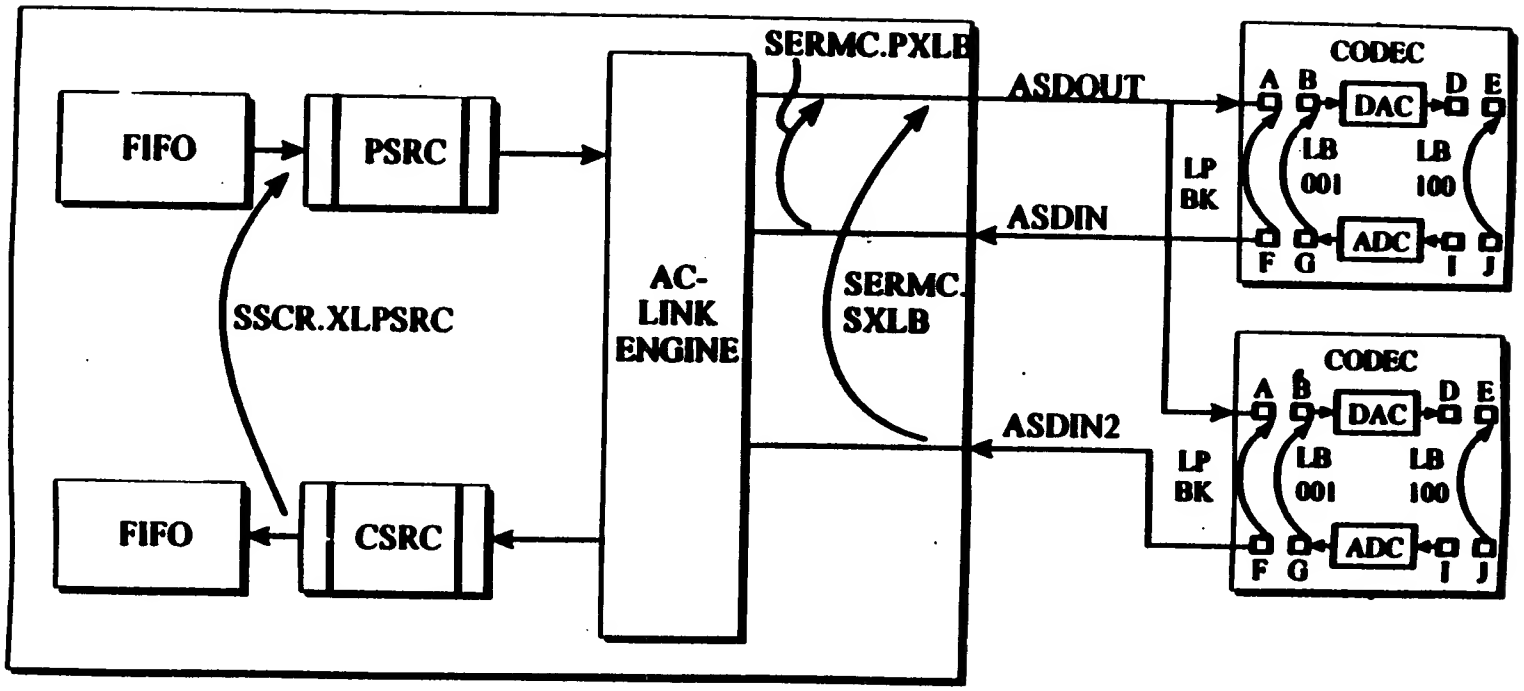


Fig. 11C

05-2401

006090 6597 6560

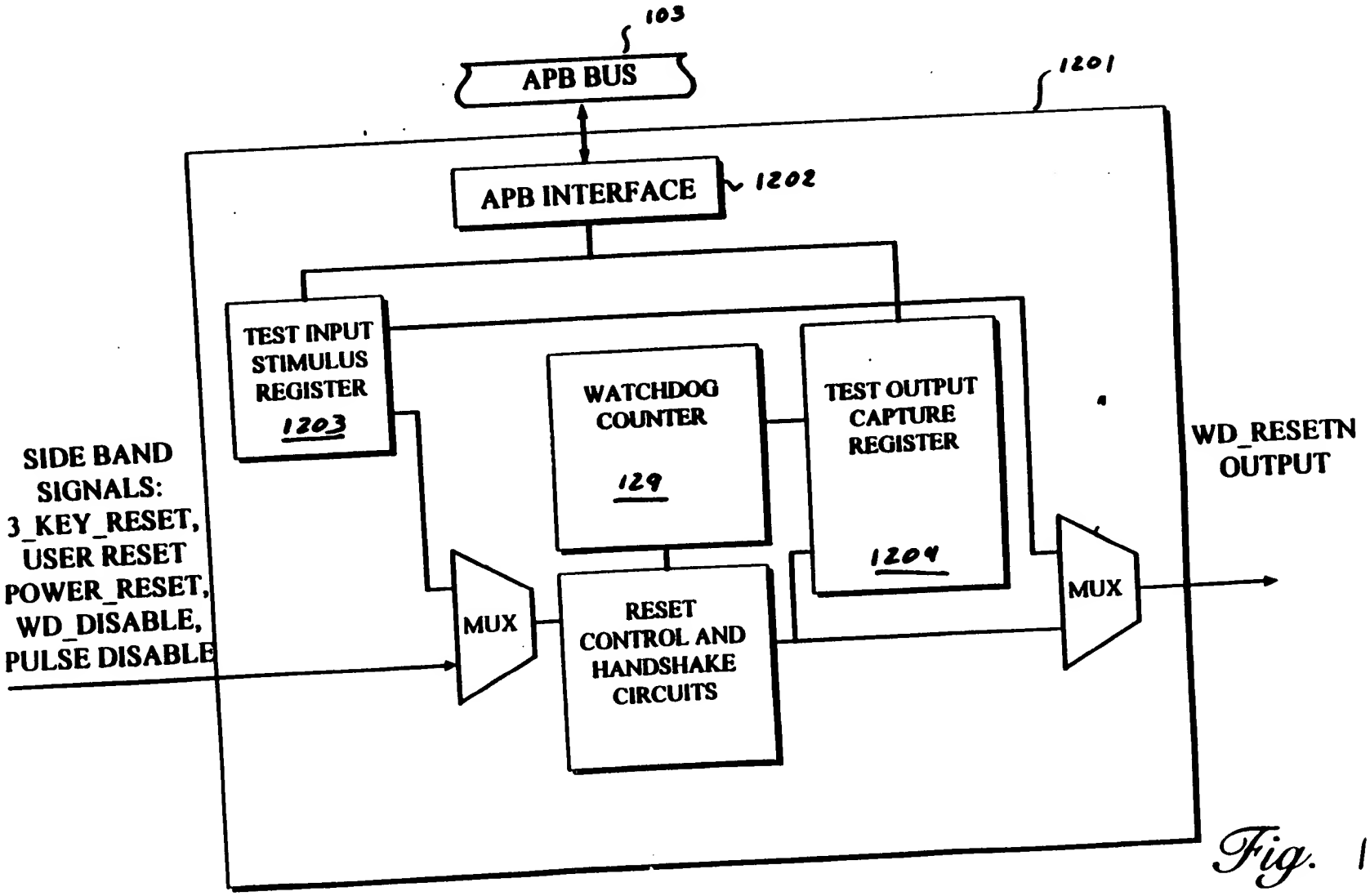


Fig. 12

d3-2601

006090 "659T6560

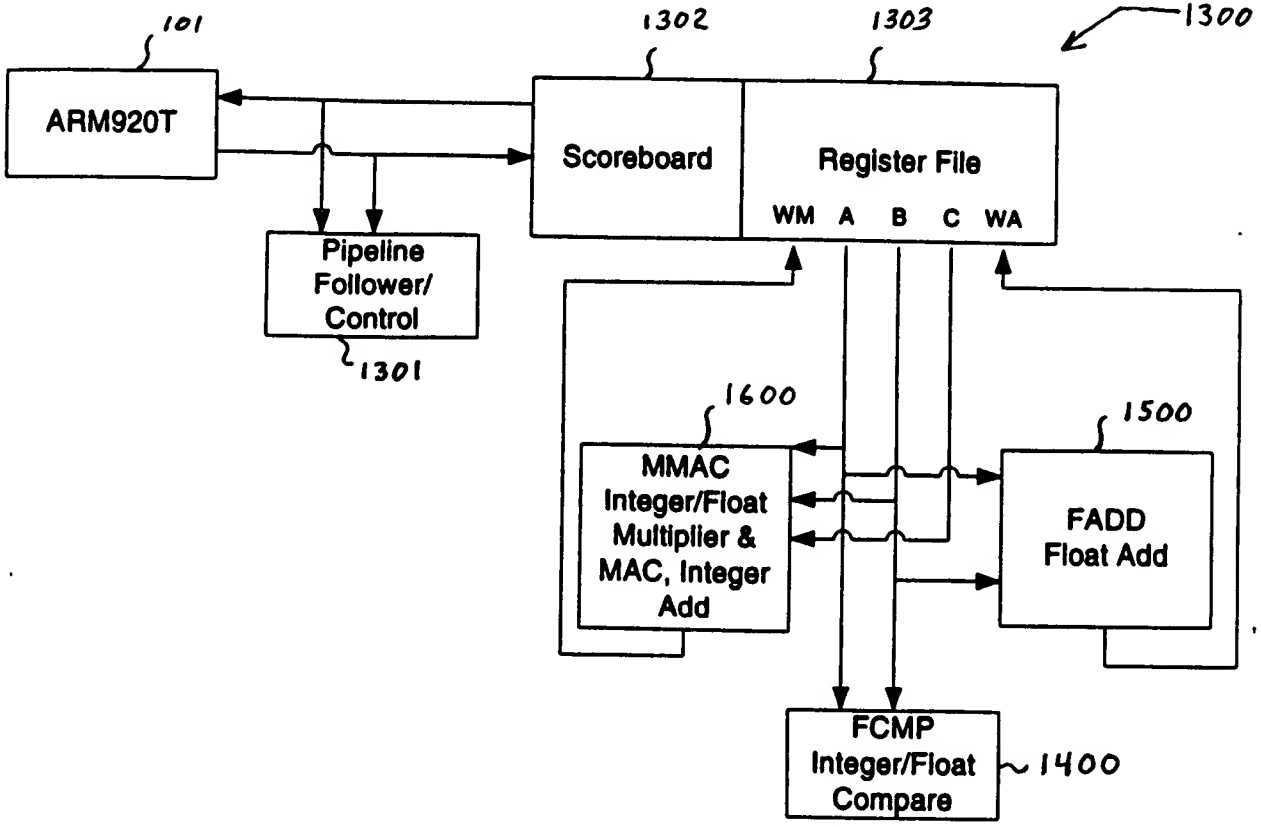


FIG. 13

10421

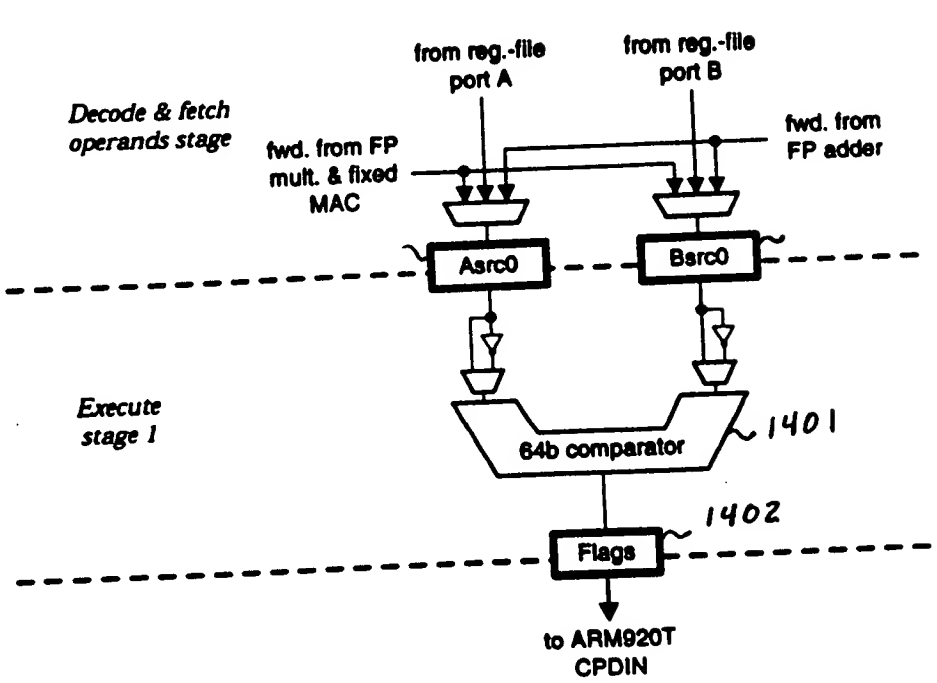

1400
from reg.-file port A
from reg.-file port B
Decode & fetch operands stage
fwd. from FP mult. & fixed MAC
fwd. from FP adder
Asrc0
Bsrc0
Execute stage 1
64b comparator
1401
1402
Flags
to ARM920T CPDIN

FIG. 14

1042-EP

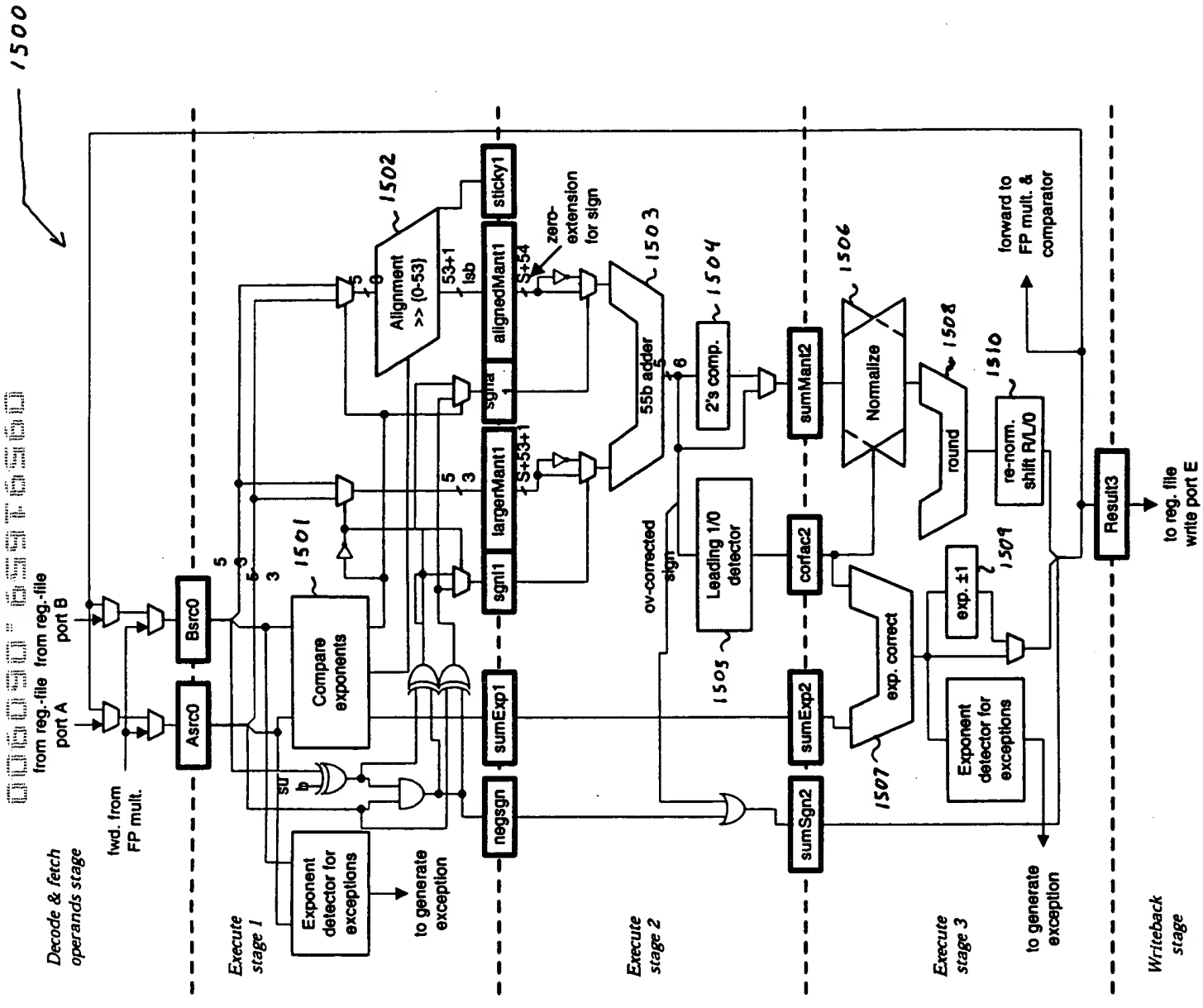


FIG. 15

1042-EP

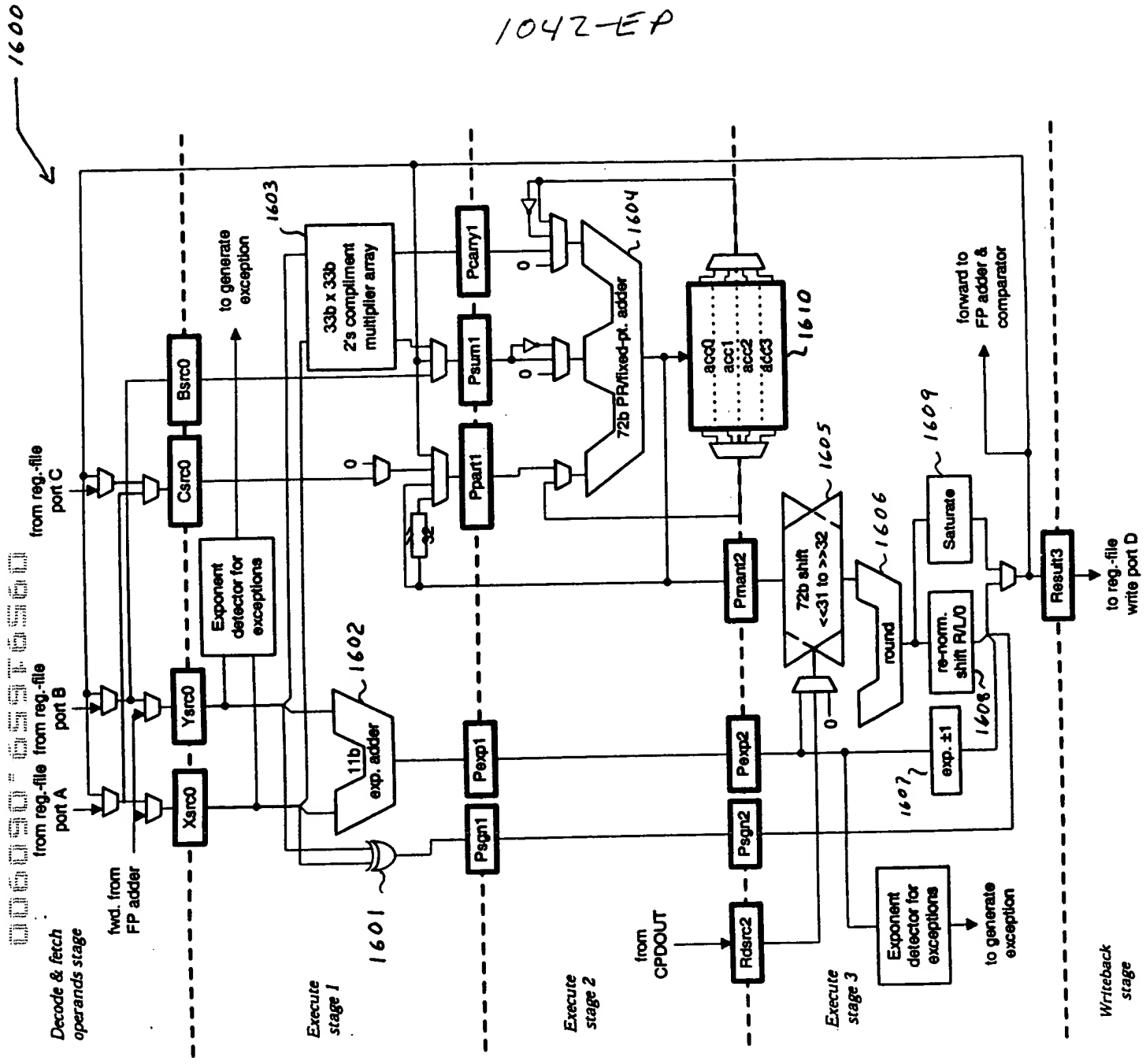


FIG. 16

Fig. 17
(sheet 1)

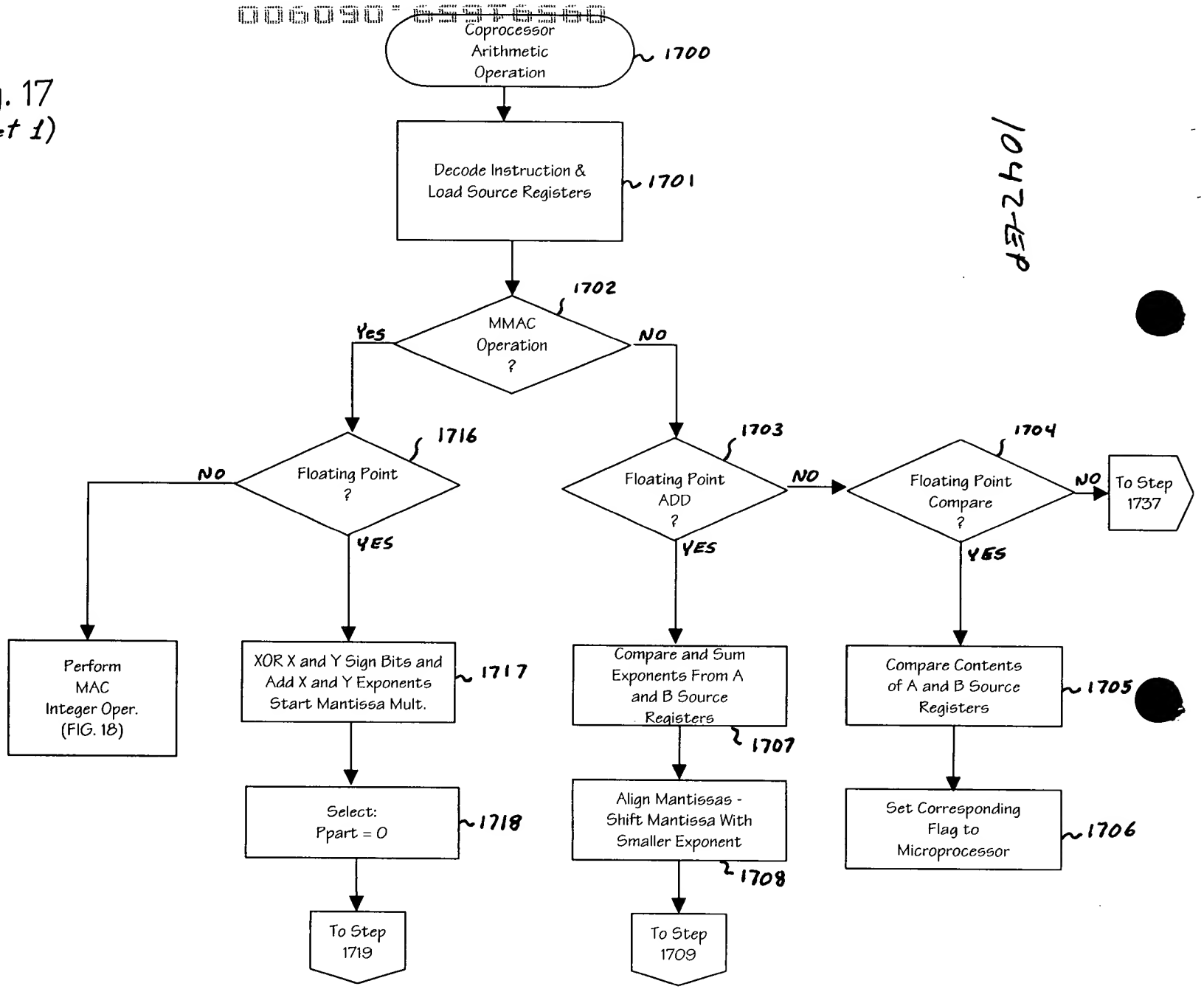
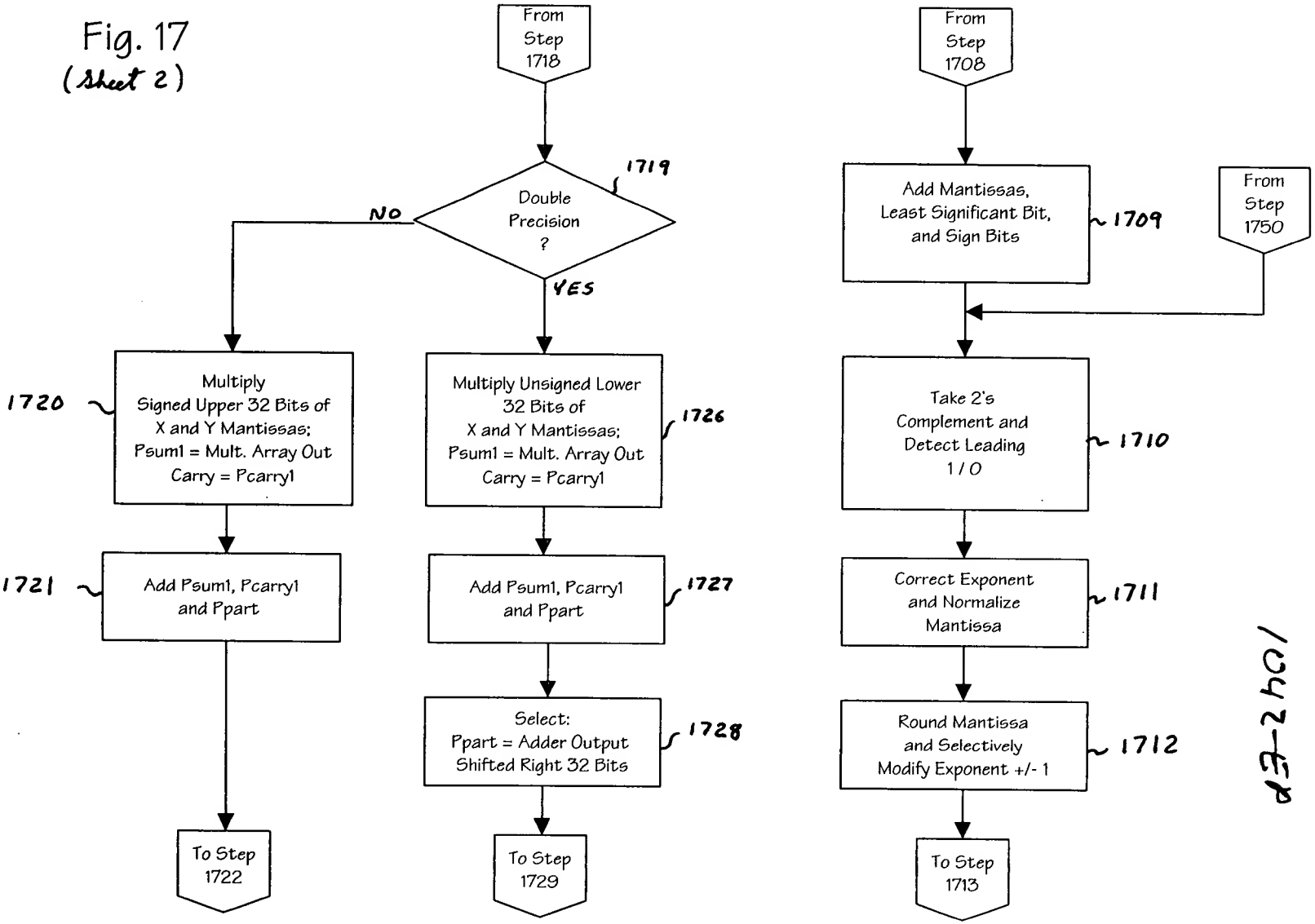


Fig. 17
(Sheet 2)



42-2601

DELL 90 69T6560

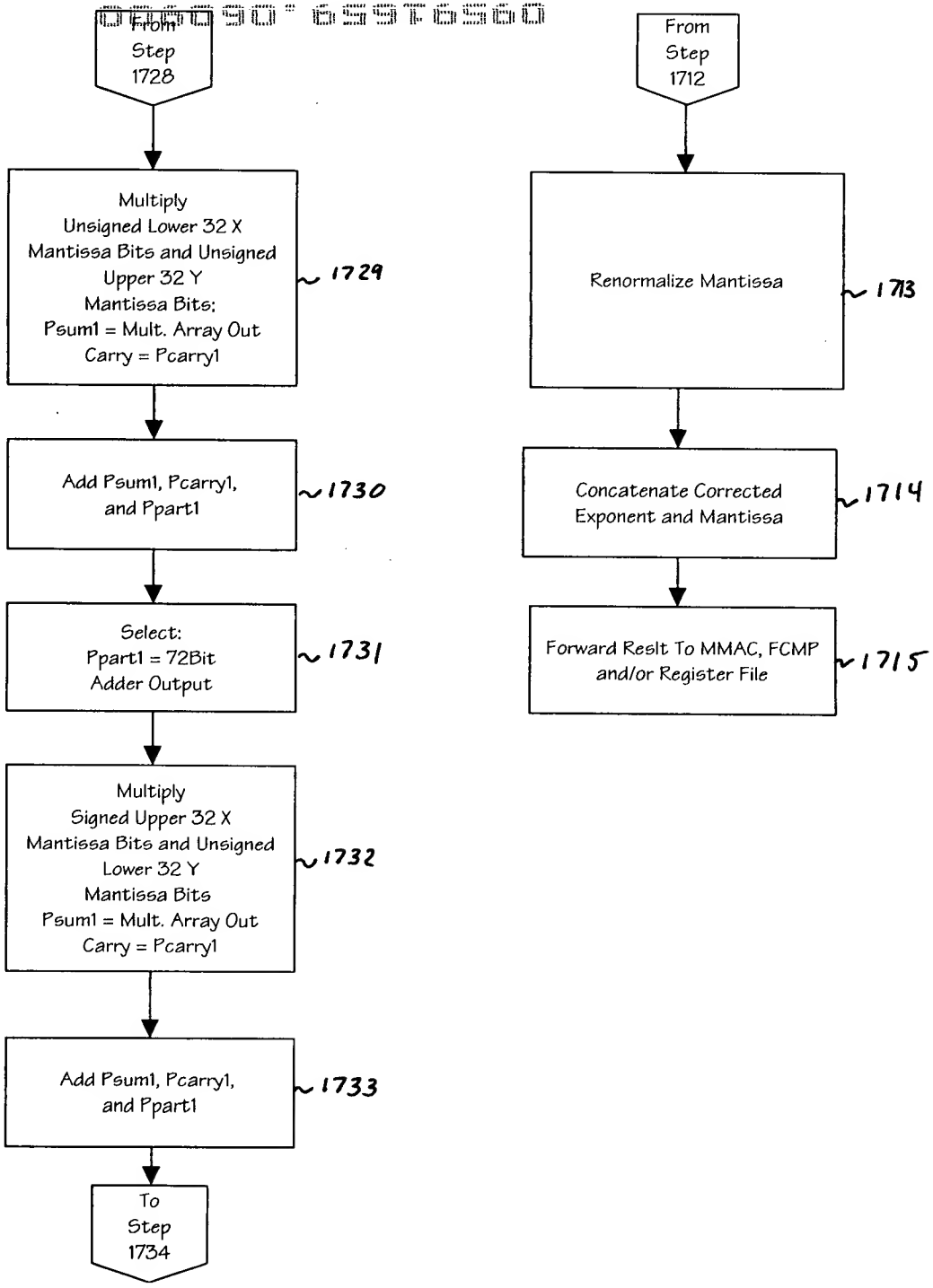


Fig. 17
(Sheet 3)

1042-50

0060901 6571650

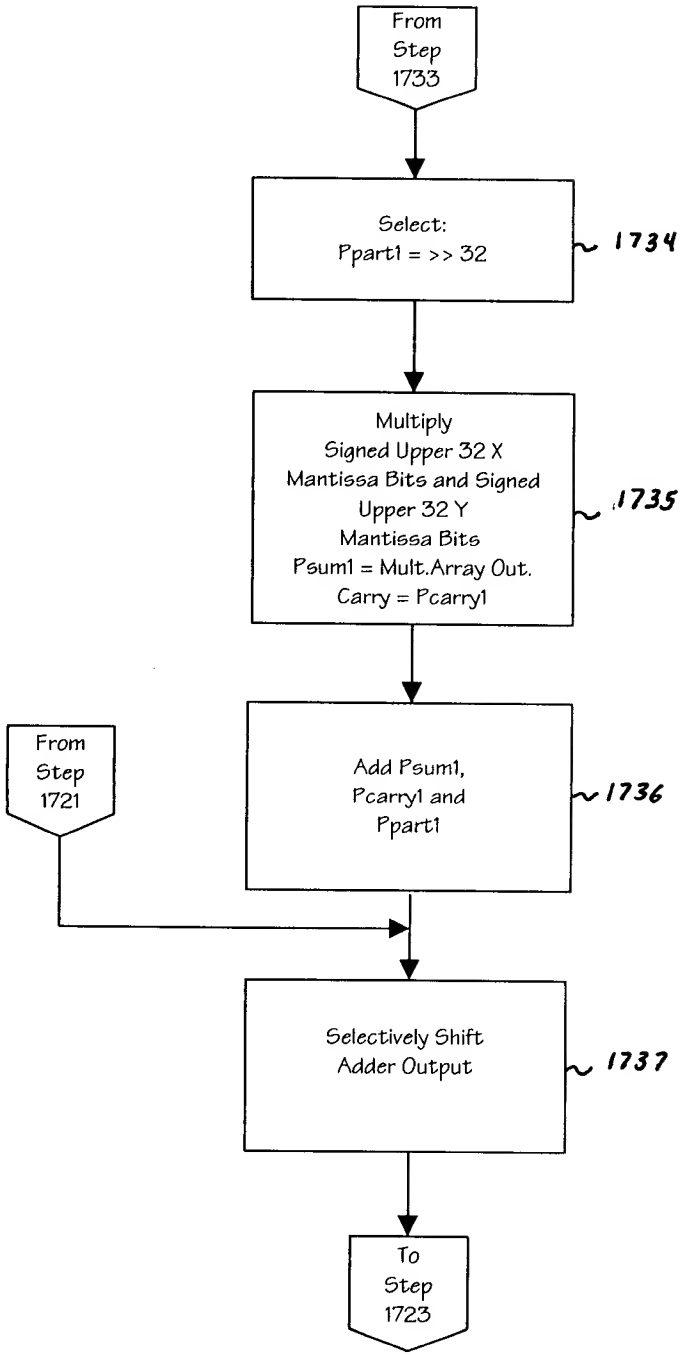


Fig. 17
(Sheet 4)

97-24701

US006058409A

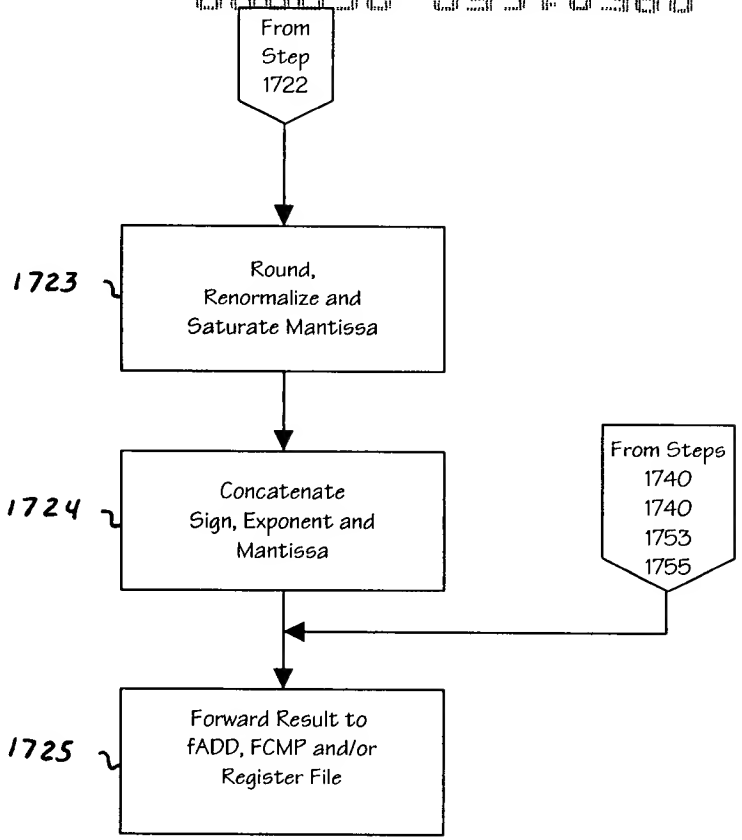
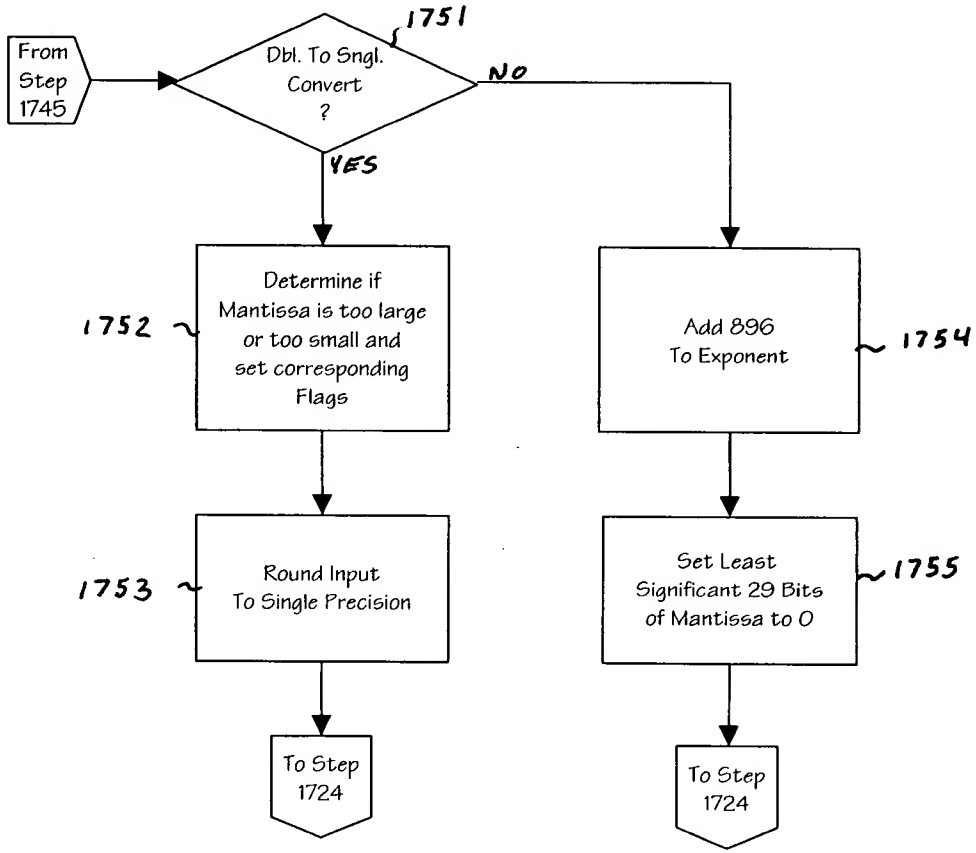
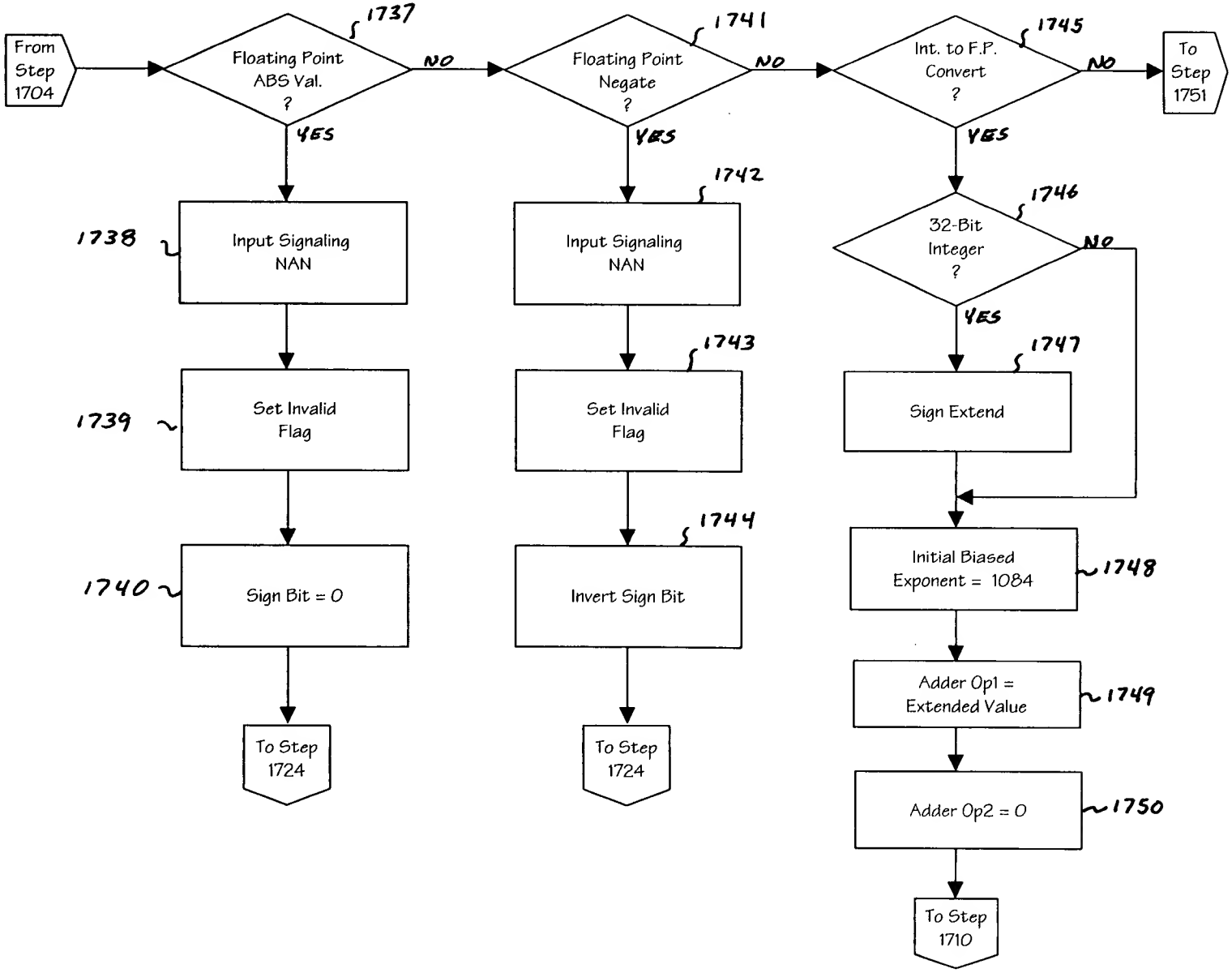


Fig. 17
(Sheet 5)

04-2401

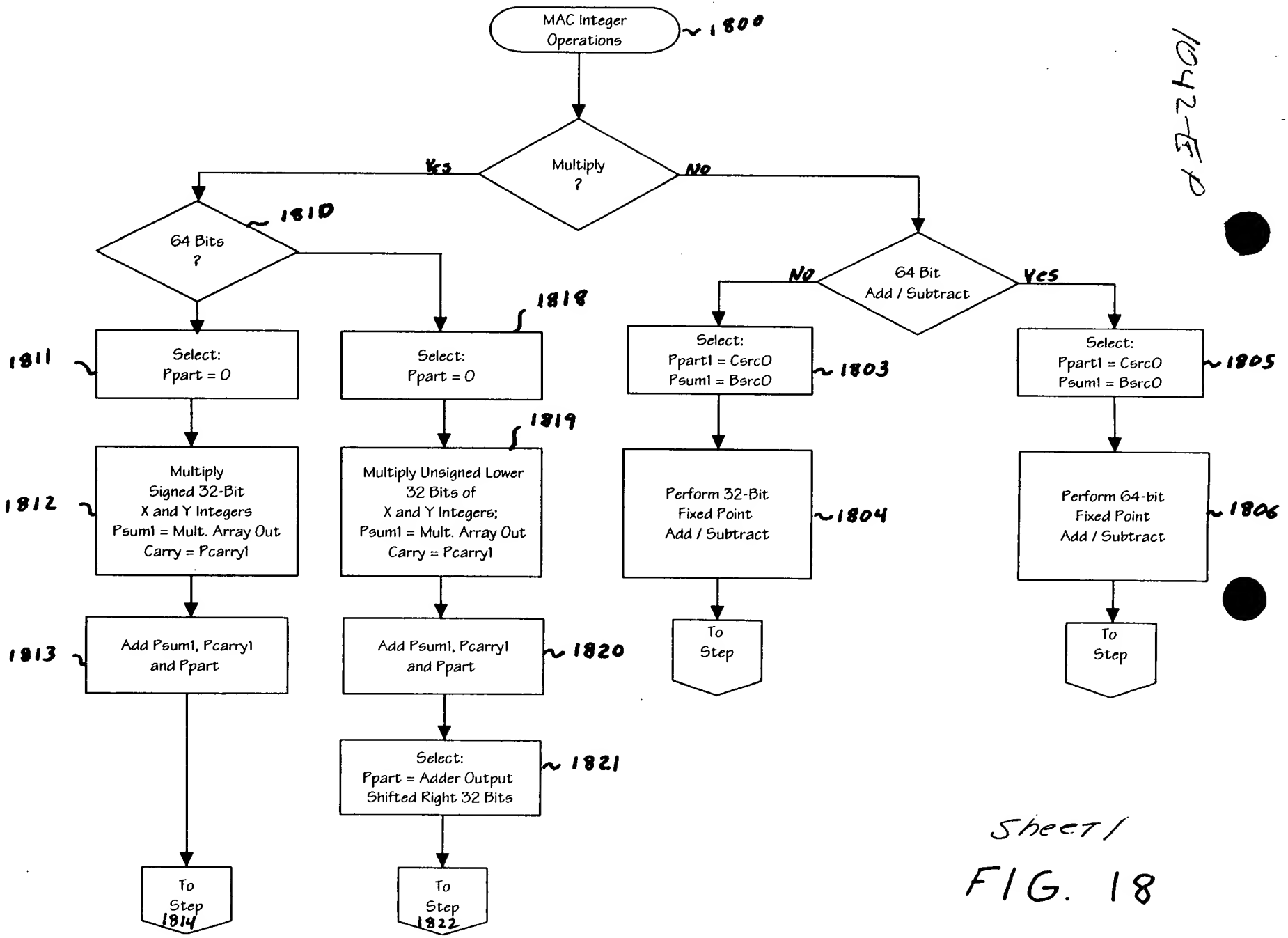
Fig. 17
(Sheet 7)





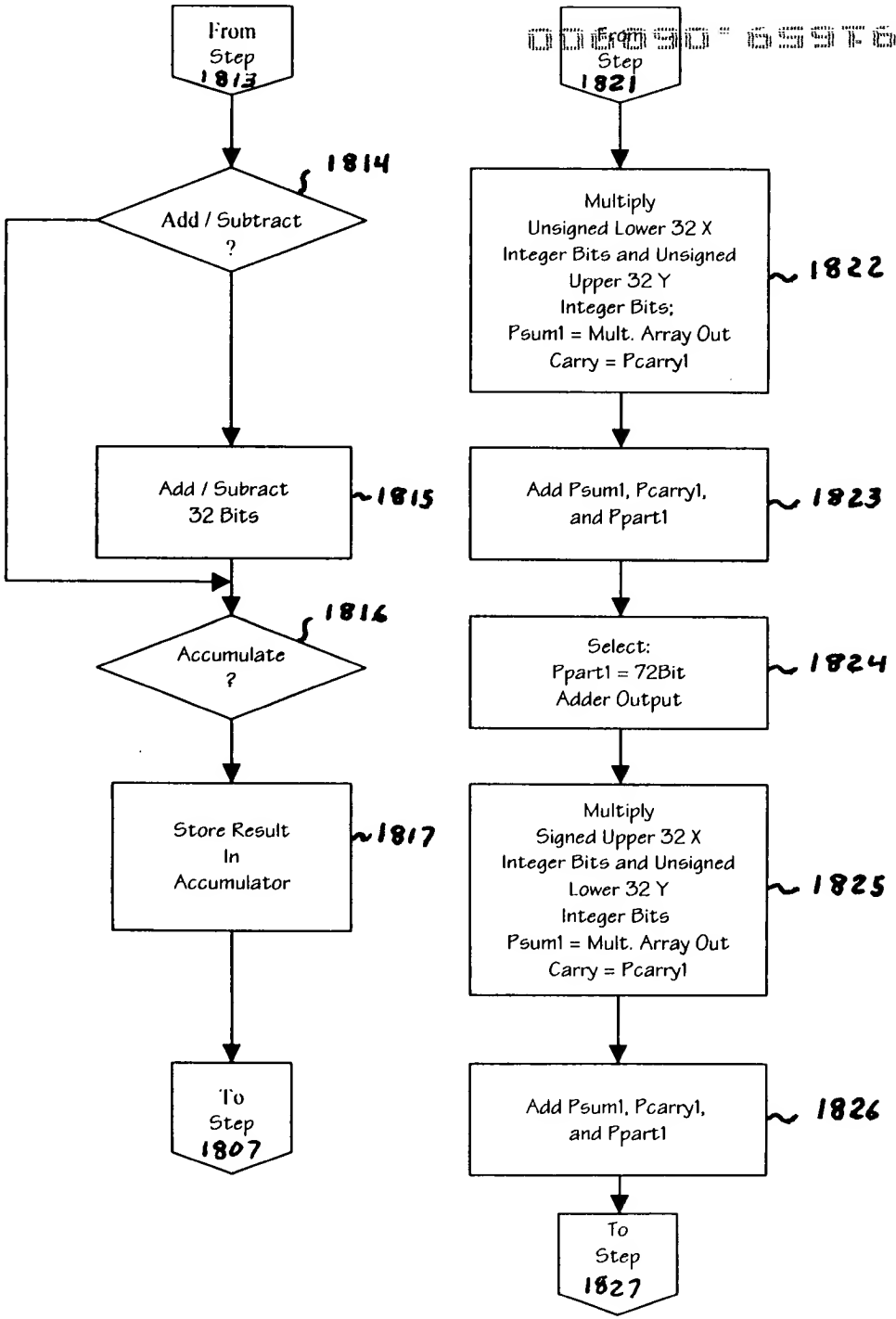
1042-EP

Fig. 17
(Sheet 6)



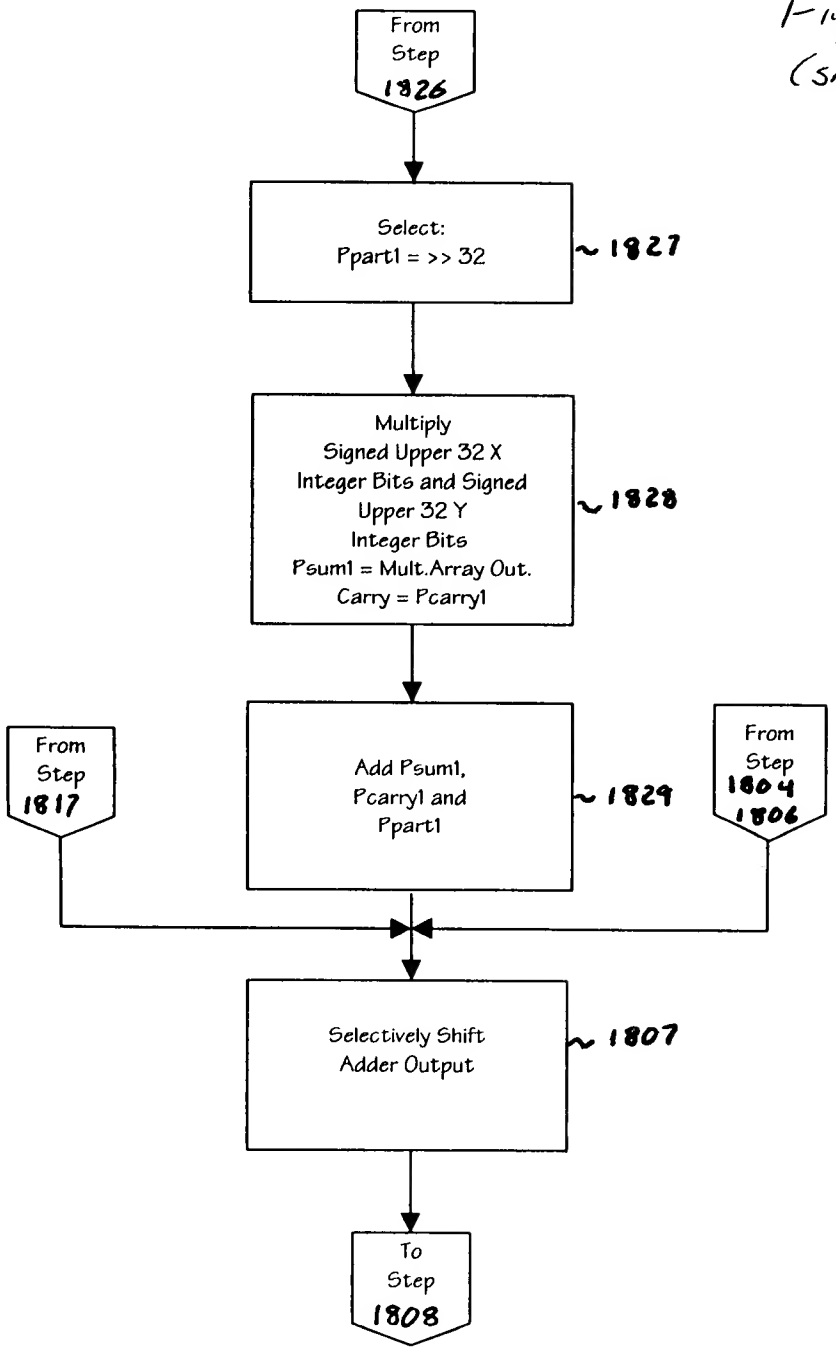
Sheet 1

FIG. 18


From Step 1813
1814
Add / Subtract ?
Add / Subract 32 Bits
1815
1816
Accumulate ?
Store Result In Accumulator
1817
To Step 1807
From Step 1821
Multiply Unsigned Lower 32 X Integer Bits and Unsigned Upper 32 Y Integer Bits; Psum1 = Mult. Array Out Carry = Pcarry1
1822
Add Psum1, Pcarry1, and Ppart1
1823
Select: Ppart1 = 72Bit Adder Output
1824
Multiply Signed Upper 32 X Integer Bits and Unsigned Lower 32 Y Integer Bits Psum1 = Mult. Array Out Carry = Pcarry1
1825
Add Psum1, Pcarry1, and Ppart1
1826
To Step 1827

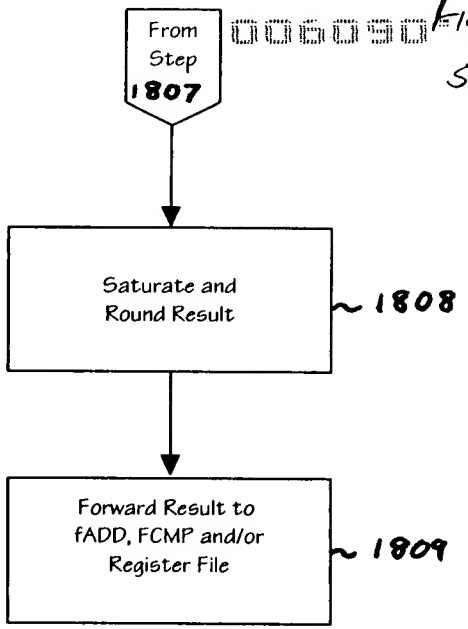
10421-E01

Fig. 18
(sheet 3)



1042-25P

Fig. 18
Sheet 4



042-EP